Introduction to Analog Design in Submicron CMOS Technologies

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The MOST important thing...

... is that you understand!

So do not hesitate to ask questions if something is not clear to you!
A second tip...

\[ \overline{t_n^2} = \frac{4kT}{R} \cdot \Delta f \]

\[ P_{av} = \lim_{T} \frac{1}{T} \int_{-T/2}^{T/2} x^2(t)dt \]

\[ f_{max} = \frac{1}{2\pi C_{gs}} \]

\[ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sRC} \]

\[ \overline{v_{in}}^{2} = 4kTn_{\gamma} \frac{1}{g_{m}} + \frac{K_{s}}{C_{ox}WL} f^{a} \]

\[ I_{DS} = I_{D0} \frac{W}{L} e^{\frac{V_{GS}}{n_{\phi t}}} (1 - e^{\frac{V_{DS}}{n_{\phi t}}}) \]

\[ p(x) = \frac{1}{\sigma \sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \]

I.C. = \frac{I_{DS}}{2n\beta\phi_{t}^{2}}

L = \mu \cdot n^{2} \cdot F(d) \cdot d

\mu = \frac{\mu_{0}}{1 + \theta (V_{GS} - V_{T})}

\phi_{t} = \frac{kT}{q}

E_{n} = \frac{-Z^{2}m_{0}q^{4}}{8\varepsilon_{0}^{2}h^{2}n^{2}}

\sigma_{\Delta V_{th}} = \text{Const} \cdot \frac{t_{ox} \cdot 4\sqrt{N}}{\sqrt{WL}}

Do not be afraid of formulas!
They are very useful tools for making good analog design

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The last warning before we start

The transparencies I will show you are sometimes quite full of details. You will not have the time to “digest” all these details this week, but I wanted to prepare the transparencies so that you will have a COMPLETE material for future reference.

During the presentation, I will help you in identifying in the transparencies and in the formulas the most important issues that you should retain.

I also made a special effort in referencing all the sources (books and papers) I have been using when preparing the lectures. This should help you in finding easily what you do not find in the transparencies...
Outline

- Semiconductor physics
  - Silicon and silicon dioxide properties
  - Band diagram concept
  - Intrinsic and doped semiconductors
  - Carrier mobility in silicon
- CMOS technology: an analog designer perspective
  - The MOS transistor
  - DC characteristics
  - Important formulas
  - Small signal equivalent circuit
  - Some cross sections of real integrated circuits
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Insulators and (semi)conductors


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## Physical Properties of Si and SiO$_2$

### at room temperature (300 K)

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>SiO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic/molecular weight</td>
<td>28.09 g/mol</td>
<td>60.08 g/mol</td>
</tr>
<tr>
<td>Atoms or molecules/cm$^3$</td>
<td>$5.0 \times 10^{22}$</td>
<td>$2.3 \times 10^{22}$</td>
</tr>
<tr>
<td>Density (g/cm$^3$)</td>
<td>2.33</td>
<td>2.27</td>
</tr>
<tr>
<td>Crystal structure</td>
<td>Diamond</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Lattice constant (Å)</td>
<td>5.43</td>
<td>—</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
<td>1.12</td>
<td>8–9</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.7</td>
<td>3.9</td>
</tr>
<tr>
<td>Intrinsic carrier concentration (cm$^{-3}$)</td>
<td>$1.4 \times 10^{10}$</td>
<td>—</td>
</tr>
<tr>
<td>Carrier mobility (cm$^2$/V-s)</td>
<td>Electron: 1430</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Hole: 470</td>
<td>—</td>
</tr>
<tr>
<td>Effective density of states (cm$^{-3}$)</td>
<td>—</td>
<td>Conduction band, $N_c$: $3.2 \times 10^{19}$</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>Valence band, $N_v$: $1.8 \times 10^{19}$</td>
</tr>
<tr>
<td>Breakdown field (V/cm)</td>
<td>$3 \times 10^5$</td>
<td>$&gt;10^7$</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>1415</td>
<td>1600–1700</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm$^2$°C)</td>
<td>1.5</td>
<td>0.014</td>
</tr>
<tr>
<td>Specific heat (J/g-°C)</td>
<td>0.7</td>
<td>1.0</td>
</tr>
<tr>
<td>Thermal diffusivity (cm$^2$/s)</td>
<td>0.9</td>
<td>0.006</td>
</tr>
<tr>
<td>Thermal expansion coefficient (°C$^{-1}$)</td>
<td>$2.5 \times 10^{-6}$</td>
<td>$0.5 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Silicon crystalline structure

Orbitals filling

- $3p^2$
- $3s^2$
- $2p^6$
- $2s^2$
- $1s^2$

Diamond lattice structure

Covalent bonding

$a = 0.513$ nm for Silicon

From energy levels to bands

Allowed energy levels

\[ E_n = -\frac{Z^2 m_0 q^4}{8\varepsilon_0^2 h^2 n^2} \]

\( Z \): atomic number
\( m_0 \): free electron mass
\( q \): electron charge
\( \varepsilon_0 \): permittivity free space
\( h \): Planck’s constant
\( n \): positive integers (level number)

... putting more atoms together (and remembering Pauli’s exclusion principle)

Allowed energy band

Forbidden energy gap

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Intrinsic and doped silicon


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**Donors and acceptors**

**Intrinsic Semiconductor:** small amount of impurities compared to the thermally generated electrons and holes

**Donor level:** the allowed energy level provided by a donor is neutral when occupied by an electron and positively charged when empty

**Acceptor level:** the allowed energy level provided by an acceptor is neutral when empty (= occupied by a hole) and negatively charged when occupied by an electron (= empty)

**Carrier density vs Temperature**

N-type semiconductor

Electrons are the majority carriers

Intrinsic carrier density (= hole density)

\[ n_i^2 = N_c \cdot N_v \cdot e^{-\frac{E_g}{kT}} \]

S. M. Sze, * Semiconductor Devices, Physics and Technology*, John Wiley and Sons, 1985, p. 27

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Mobility vs T and $N_D$

$N_D$: doping concentration

$$v_d = -\frac{q\tau_m}{m_e}E = -\mu_nE$$

$v_d$ = drift velocity

$\tau_m$ = mean free time between collisions

$m_e$ = conductivity effective mass

$E$ = electric field

Mobility vs doping

\[ \frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I} + \frac{1}{\mu_S} \]

\( \mu = \text{total mobility} \)
\( \mu_L = \text{mobility due to lattice scattering} \)
\( \mu_I = \text{mobility due to impurity scattering} \)
\( \mu_S = \text{mobility due to surface scattering (the dominating factor in MOS transistors)} \)

It is like for resistors in parallel: the smaller dominates!


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Carrier velocity vs Electric Field

Resistivity vs doping

\[ \rho = \frac{1}{q(n\mu_n + p\mu_p)} \]

- \( q \) = electronic charge
- \( \rho \) = resistivity
- \( n, p \) = carrier concentration
- \( \mu_n, \mu_p \) = carrier mobility

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The MOS transistor

\[ i_{DS} = g_m \cdot v_{GS} \]

Transconductance

CMOS technology

NMOS

PMOS

sub S G D S G D well

p+ n+ n+ p+ p+ n+

p-substrate n-well

Polysilicon Oxide Electrons Holes

n+ source n+ drain

NMOS layout

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LINEAR REGION (Low $V_{DS}$): Electrons (in light blue) are attracted to the SiO$_2$ – Si Interface. A conductive channel is created between source and drain. We have a Voltage Controlled Resistor (VCR).

SATURATION REGION (High $V_{DS}$): When the drain voltage is high enough the electrons near the drain are insufficiently attracted by the gate, and the channel is pinched off. We have a Voltage Controlled Current Source (VCCS).
Drain current vs Drain voltage

![Graph showing Drain current (I_DS) vs Drain voltage (V_DS) with regions labeled: Saturation region (VCCS), Linear region (VCR), and Locus of I_DS_SAT vs V_DS_SAT.](image)

- **Saturation region (VCCS)**
- **Linear region (VCR)**
- **Locus of I_DS_SAT vs V_DS_SAT**

@ three different V_{GS}
Equations: strong inversion

**LINEAR REGION:**

\[ V_{DS} < \frac{V_{GS} - V_T}{n} = V_{DS\_SAT} \]

\[ I_{DS} = \beta \left( V_{GS} - V_T - \frac{nV_{DS}}{2} \right) V_{DS} \]

Transconductance: \( g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta V_{DS} \)

**SATURATION REGION:**

\[ V_{DS} > \frac{V_{GS} - V_T}{n} = V_{DS\_SAT} \]

\[ I_{DS} = \frac{\beta}{2n} (V_{GS} - V_T)^2 \]

Transconductance: \( g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\beta}{n} (V_{GS} - V_T) = \sqrt{2\frac{\beta}{n} I_{DS}} \)

\[ n = \frac{g_m + g_{mb}}{g_m} \approx 1.x \quad g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} \quad \beta = \mu C_{ox} \frac{W}{L} \quad C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}} \]
Drain current vs Gate voltage

Subthreshold region

Linear region (green) and saturation region (red)

High field (vertical and longitudinal) effects

VGS [V]

IDS [A]
Log($I_{DS}$) vs $V_{GS}$
Equations: weak inversion

\[ I_{DS} = I_{D0} \frac{W}{L} e^{\frac{v_{GS}}{n\phi_t}} \left( 1 - e^{\frac{v_{DS}}{n\phi_t}} \right) \]

If \( V_{DS} > 4n\phi_t \), then the drain current does not depend on \( V_{DS} \) any longer (saturation).

\[ I_{DS} = I_{D0} \frac{W}{L} e^{\frac{v_{GS}}{n\phi_t}} \]

\[ g_m = \frac{\partial I_{DS}}{\partial v_{GS}} = \frac{I_{DS}}{n\phi_t} \]

Almost like a bipolar transistor!

\[ \phi_t = \frac{kT}{q} \approx 25 \text{ mV @ 300 K} \]
Transcond. vs Gate voltage

Measurement made in the linear region.
Output conductance

\[ G_{\text{out}} = \frac{\Delta I}{\Delta V} = \frac{I_D}{\Delta V} \cdot \frac{\Delta L}{L - \Delta L} \]

Dashed lines: ideal behavior

\[ V_{DS} \ [\text{V}] \]
\[ I_{DS} \ [\text{A}] \]

\[ S \quad G \quad D \]
\[ n^+ \quad \Delta L \quad n^+ \]

\[ V_{D}, V_{D'}, V_{DS} \]

\[ \Delta V \quad \Delta I \]
Equations: output conductance

\[ I_{DS} = \frac{\beta}{2n} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ V_{DS \_SAT} = \frac{V_{GS} - V_T}{n} \]

\[ I_{DS \_SAT} = \frac{\beta}{2n} (V_{GS} - V_T)^2 = \frac{\beta}{2} n V_{DS \_SAT}^2 \]

\[ g_{out} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \lambda \cdot I_{DS \_SAT} \]

\[ r_0 = \frac{1}{g_{ds}} = \frac{1}{\lambda \cdot I_{DS \_SAT}} = \frac{V_E \cdot L}{I_{DS \_SAT}} \]

\[ \lambda = \frac{1}{V_{DS}} \cdot \frac{\Delta L}{L - \Delta L} \quad \text{where} \quad \Delta L = f(V_{DS}, N_{Doping}) \]
Equations: addendum

Bulk effect
\[ \Delta V_T = \gamma \cdot \left( \sqrt{V_{sb}} + \phi_{Si} - \phi_{Si} \right) \]
\[ \gamma = \frac{\sqrt{2q\varepsilon_{Si}N_a}}{C_{ox}} \]

Source parasitic resistance
\[ g'_m = \frac{g_m}{1 + g_m R_s} \]

Vertical electric field effect
\[ \mu = \frac{\mu_0}{1 + \theta (V_{GS} - V_T)} \]

Maximum frequency
\[ f_{max} = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = \frac{1}{2\pi} \frac{\mu}{nL^2} (V_{GS} - V_T) \] in s.i.

Equations: velocity saturation

For low values of the longitudinal electric field, the velocity of the carriers increases proportionally to the electric field (and the proportionality constant is the mobility). For high values of the electric field (3 V/\( \mu \)m for electrons and 10 V/\( \mu \)m for holes) the velocity of the carriers saturates.

\[
I_{DS\_V.S.} = W C_{ox} v_{sat} (V_{GS} - V_{T}) \quad \text{with} \quad v_{sat} = 10^7 \frac{\text{cm}}{\text{s}}
\]

\[
g_{m\_V.S.} = W C_{ox} v_{sat}
\]

\[
f_{max\_V.S.} = \frac{1}{2\pi} \frac{g_m}{C_{gs}} = \frac{1}{2\pi} \frac{v_{sat}}{L}
\]
\( g_m / I_D \ vs \ \log(I_D / W) \)

**Weak Inversion (W.I.)**

\[
g_m = \frac{I_{DS}}{n \phi_t} \quad \rightarrow \quad \frac{g_m}{I_D} = \frac{1}{n \phi_t}
\]

**Strong Inversion (S.I.)**

\[
g_m = \sqrt{2 \frac{\beta}{n} I_{DS}} \quad \rightarrow \quad \frac{g_m}{I_D} = \sqrt{2 \frac{\beta}{n} \frac{1}{I_{DS}}}
\]

**Velocity Saturation (V.S.)**

\[
g_m = WC_{ox} v_{sat} \quad \rightarrow \quad \frac{g_m}{I_{DS}} = \frac{WC_{ox} v_{sat}}{I_{DS}}
\]
Log($g_m / I_D$) vs log($I_D / W$)

Slope = -0.5
Strong inversion

Slope = -1
Velocity saturation
The poor PMOS transistor

\[ I_{DS} = -\frac{\beta}{2n} (V_{GS} - V_T)^2 \]

\[ g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \]

\[ = -\frac{\beta}{n} (V_{GS} - V_T) = \]

\[ = \sqrt{-2\frac{\beta}{n} I_{DS}} \]

\[ V_T < 0 \text{ V} \]
\[ V_{GS} < 0 \text{ V} \]
\[ I_{DS} < 0 \text{ V} \]
Small-signal equivalent circuit

This equation fixes the bias point

\[
I_{DSQ} = \frac{\beta}{2n} (V_{GSQ} - V_T)^2
\]

This equation defines the small signal behavior

\[
I_{DS} = g_m \cdot V_{GS}
\]

Small-signal equivalent circuit
The real thing!

SOI technology from IBM


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The real thing!

Metallization examples


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Why is CMOS so widespread?

- The IC market is driven by digital circuits (memories, microprocessors, …)
- Bipolar logic and NMOS - only logic had a too high power consumption per gate
- Progress in the manufacturing technology made CMOS technologies a reality
- Modern CMOS technologies offer excellent performance (especially for digital): high speed, low power consumption, VLSI, low cost, high yield

CMOS technologies occupies an increasing portion of the IC market

… and this is why we will only talk about CMOS.
The next three lectures

- Lecture 2: Noise and Matching in CMOS (Analog) Circuits
- Lecture 3: Scaling Impact on Analog Circuit Performance
- Lecture 4: Basic Building Blocks for Analog Design