

Micro-electronics at CERN

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CERN, Switzerland
2008

Outline

- CERN
- LHC and its Detectors
- Electronics and the Physics experiments:
 - Electronics and radiation
 - Radiation tolerance by design
- The microelectronics Group
- LHC projects:
 - Timing & Time measurements:
 - Data links
 - Experiment control
 - Frontend electronics
- Medical applications

CERN - European Organization for Nuclear Research

- Conseil Européen pour la Recherche Nucléaire
- The concept of an "European Science Laboratory" was first proposed by Louis de Broglie in 1949
- UNESCO "subscribes" the idea in 1950
- In 1952, 11 European governments agree to create a "provisional" CERN
- The European Organization for Nuclear Research formally comes in to being on 29 September 1954
- Today CERN counts with 20 member states

CERN - Member States

The Twenty Member States of CERN

Founding Member States (1954):

Belgium
Denmark
France
Germany
Greece
Italy
Netherlands
Norway
Sweden
Switzerland
United Kingdom
Yugoslavia (till 1961).

Member states that joined later:

1959, Austria
1961, Spain
1985, Portugal
1991, Finland and Poland
1992, Hungary
1993, Czech and Slovak Republics
1999, Bulgaria



Member States (Dates of Accession)

 AUSTRIA (1959)	 DENMARK (1953)	 GREECE (1953)	 NORWAY (1953)	 SPAIN (1/1961-12/1968-1/1983)
 BELGIUM (1953)	 FINLAND (1991)	 HUNGARY (1992)	 POLAND (1991)	 SWEDEN (1953)
 BULGARIA (1999)	 FRANCE (1953)	 ITALY (1953)	 PORTUGAL (1986)	 SWITZERLAND (1953)
 CZECH FR (1993)	 GERMANY (1953)	 NETHERLANDS (1953)	 SLOVAK FR (1993)	 UNITED KINGDOM (1953)

CERN AC/DU/MH - ES 308 1999 - 15.6.99

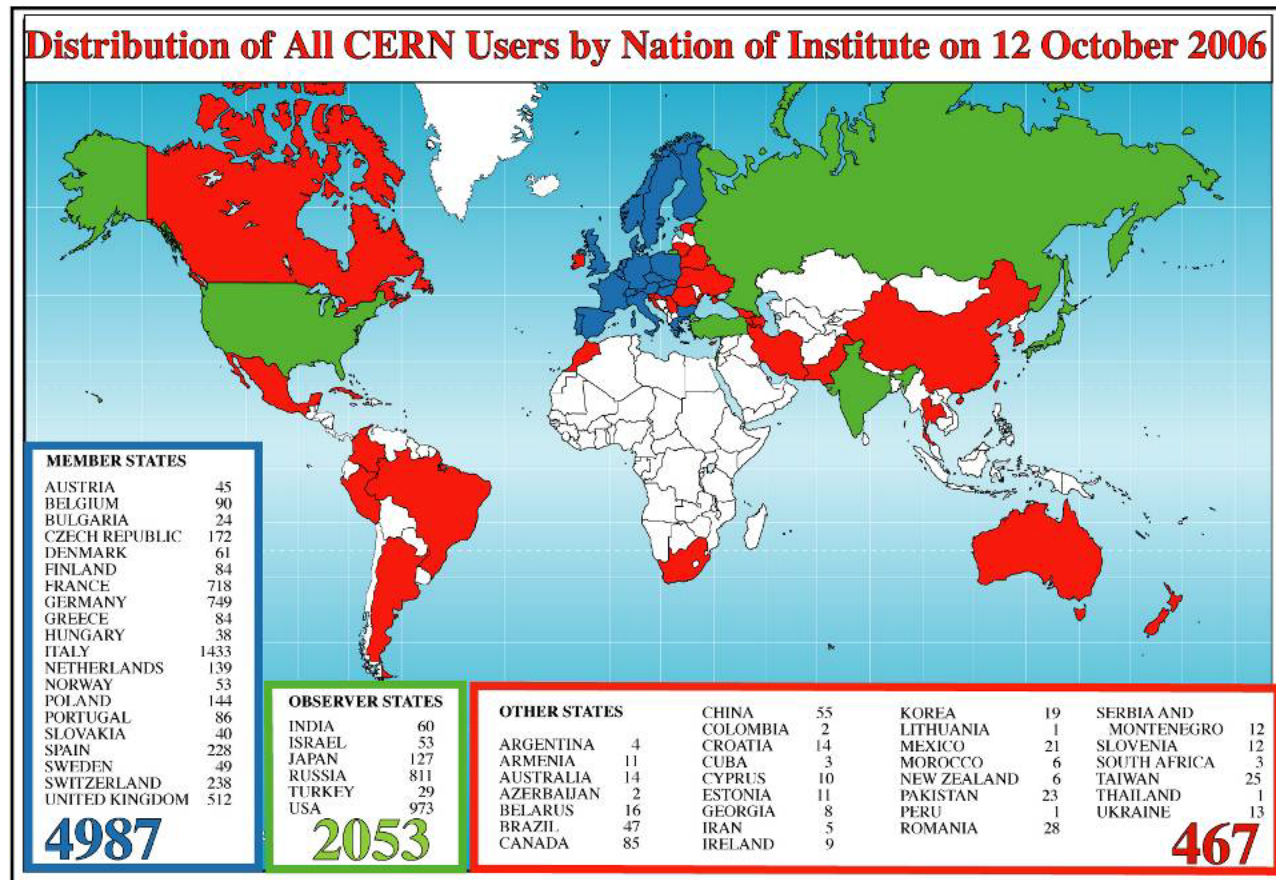
CERN - Worldwide Collaboration

CERN employs just under 3000 people:

- Physicists
- Engineers
- Technicians
- Craftsmen
- Administrators
- Secretaries
- Workmen
- ...

6500 visiting scientists representing:

- 500 Universities
- 80 Nationalities

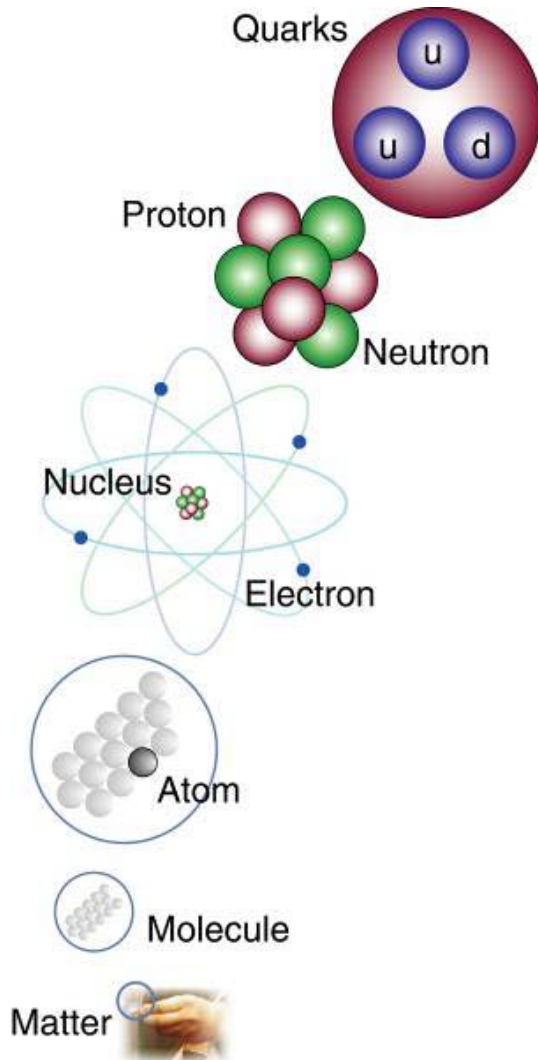


CERN - Physics Research

- The goal of physicists that work at CERN is to understand:
 - How matter is made?
 - What forces hold it together?

- CERN's mission is to provide the the infrastructures for the realization of High Energy Physics (HEP) experiments:
 - The particle accelerators
 - The particle detectors

The study of elementary particles and fields and their interactions



matter particles

	1st gen.	2nd gen.	3rd gen.
Q U A R K	<i>u</i> <i>up</i>	<i>c</i> <i>charm</i>	<i>t</i> <i>top</i>
	<i>d</i> <i>down</i>	<i>s</i> <i>strange</i>	<i>b</i> <i>bottom</i>
L E P T O N	<i>ν_e</i> <i>e neutrino</i>	<i>ν_μ</i> <i>μ neutrino</i>	<i>ν_τ</i> <i>τ neutrino</i>
	<i>e</i> <i>electron</i>	<i>μ</i> <i>muon</i>	<i>τ</i> <i>tau</i>

gauge particles

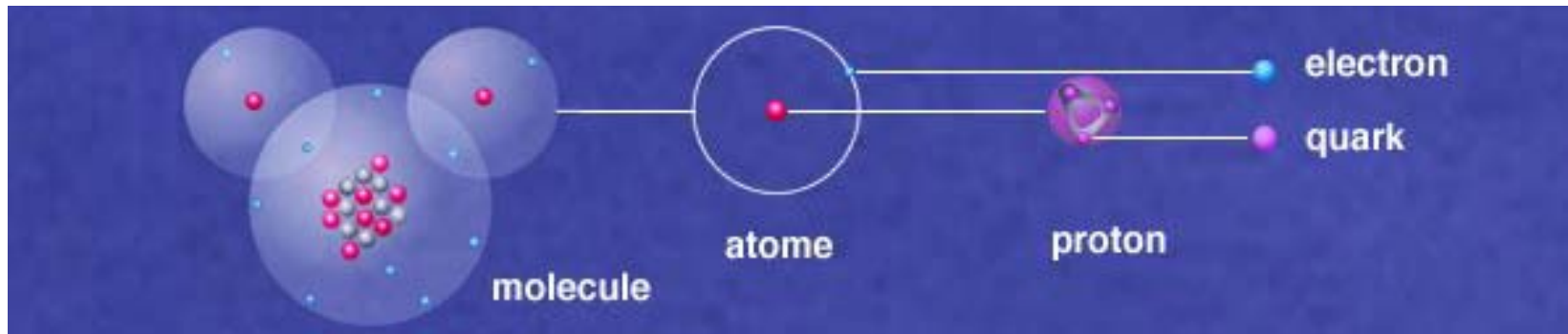
<p>Strong Force</p> <i>g</i> ×8 <i>Gluon</i>
<p>Electro-Magnetic Force</p> <i>γ</i> <i>photon</i>
<p>Weak Force</p> <i>W⁺</i> <i>W⁻</i> <i>Z</i> <i>W bosons</i> <i>Z boson</i>

scalar particle(s)

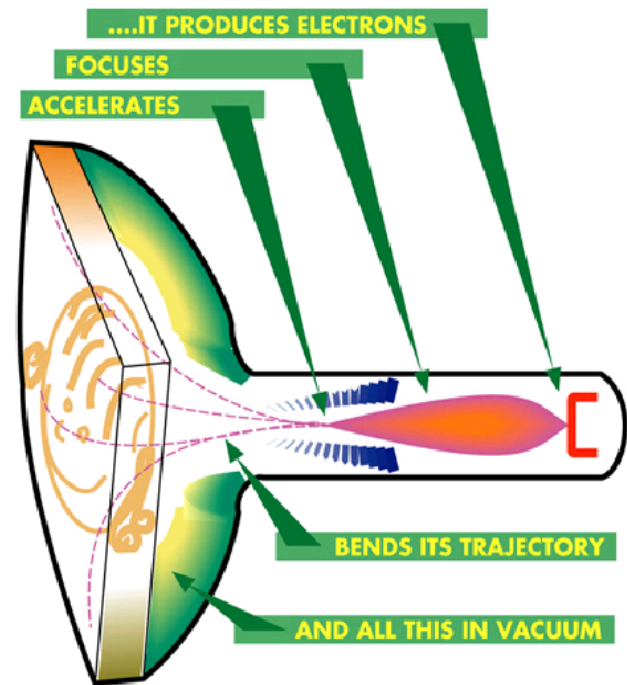


Elements of the Standard Model

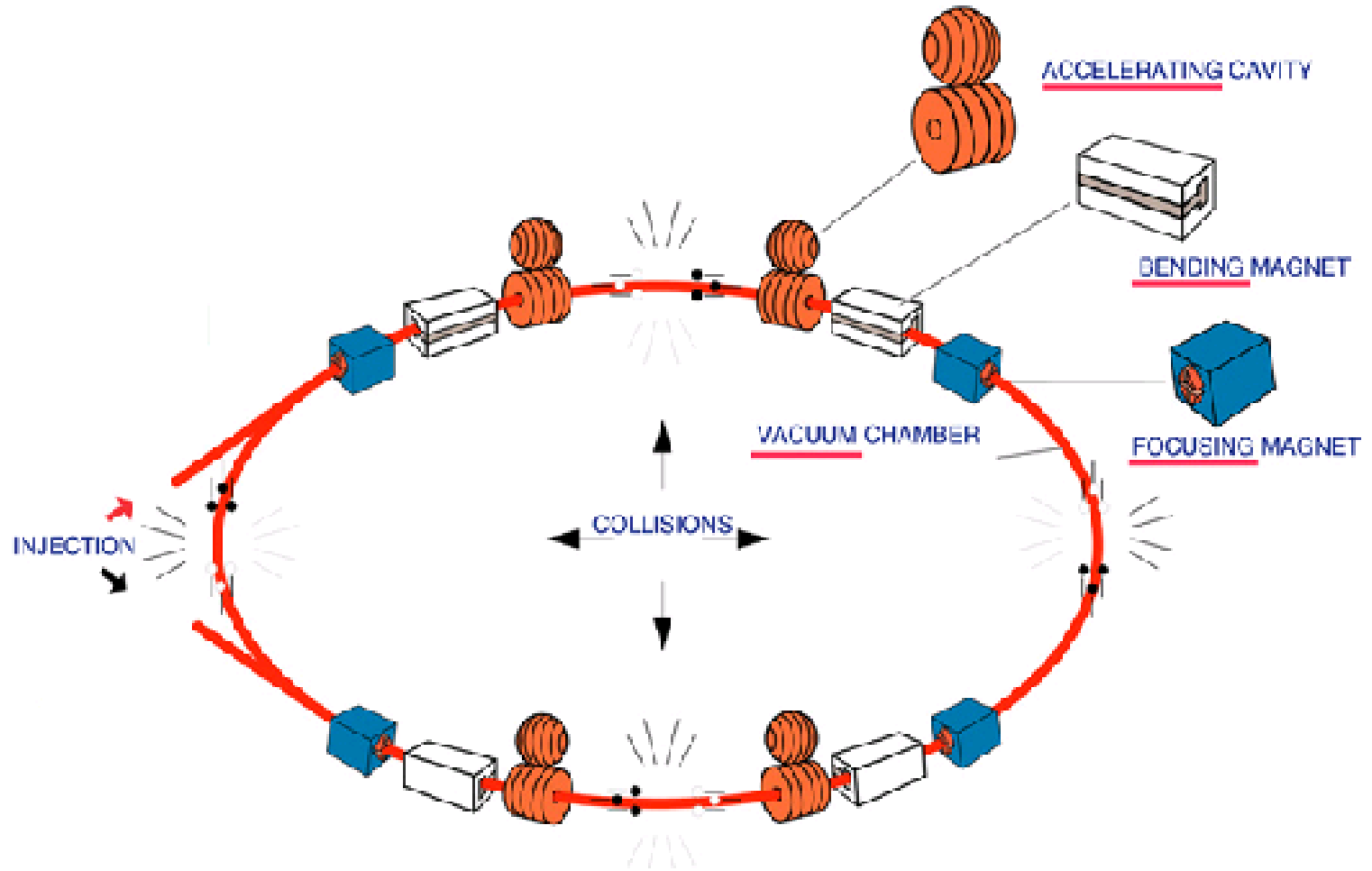
CERN - Particle Accelerators



- Like atoms, protons and neutrons also possess an internal structure.
- Physicists collide particles at high energies to reveal their internal structure.
- High energies are achieved using particle accelerators.
- The most common type of particle accelerators is the Cathode Ray Tube (most likely you have one at home).

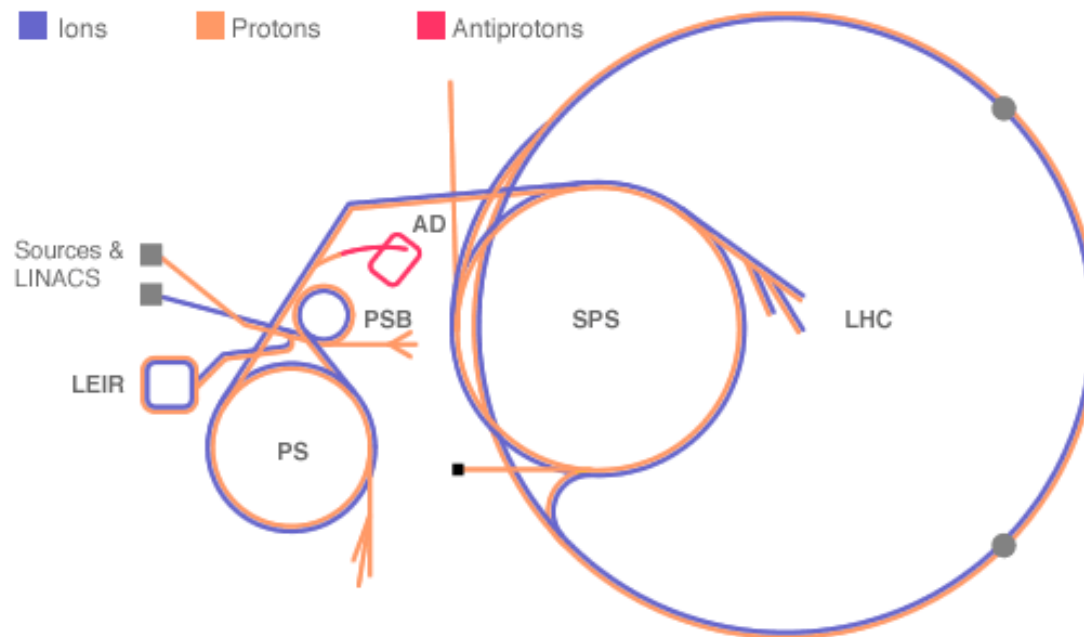


CERN - Particle Accelerators



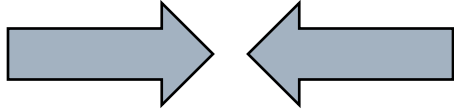
CERN - Particle Accelerators

- A succession of machines bring the beam to high energies
- The highest level of energy will be achieved in the Large Hadron Collider
 - Collide proton beams with energies around **7-on-7 TeV**
 - Collide beams of heavy ions such as lead with a total collision energy in excess of **1,250 TeV**

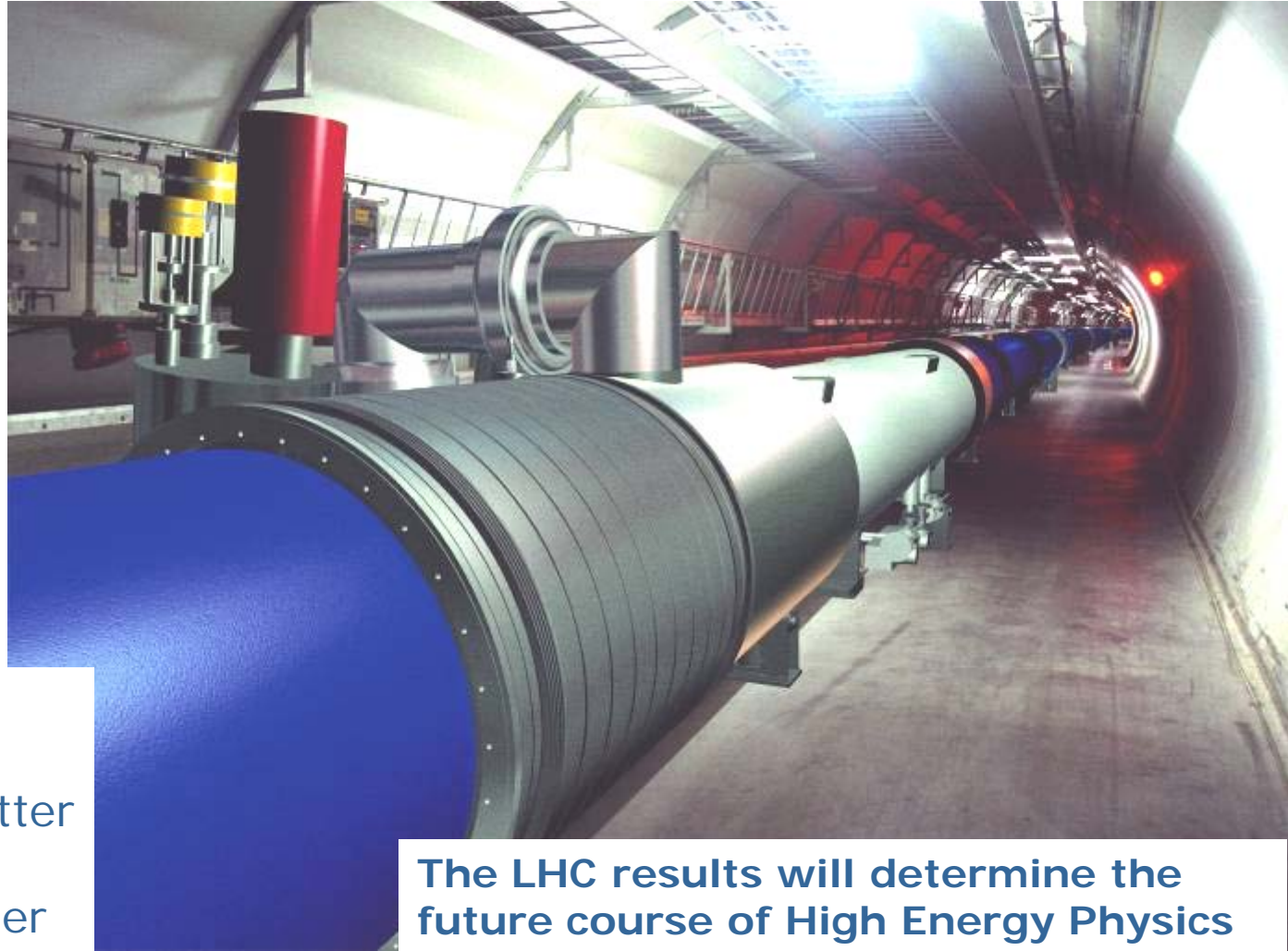


The LHC = Proton - Proton Collider

7 TeV + 7 TeV



Luminosity =
 $10^{34} \text{ cm}^{-2}\text{sec}^{-1}$

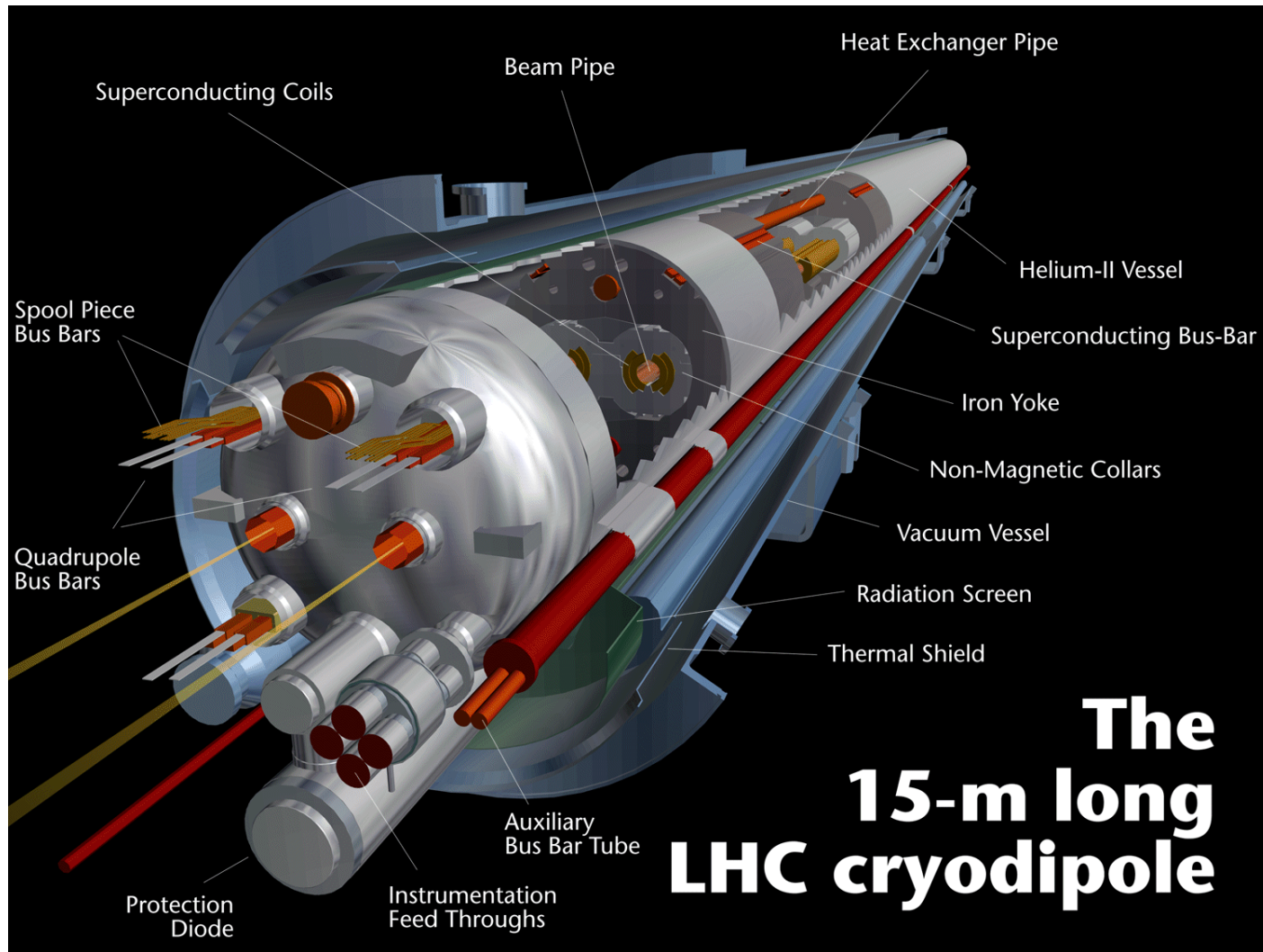


Primary targets:

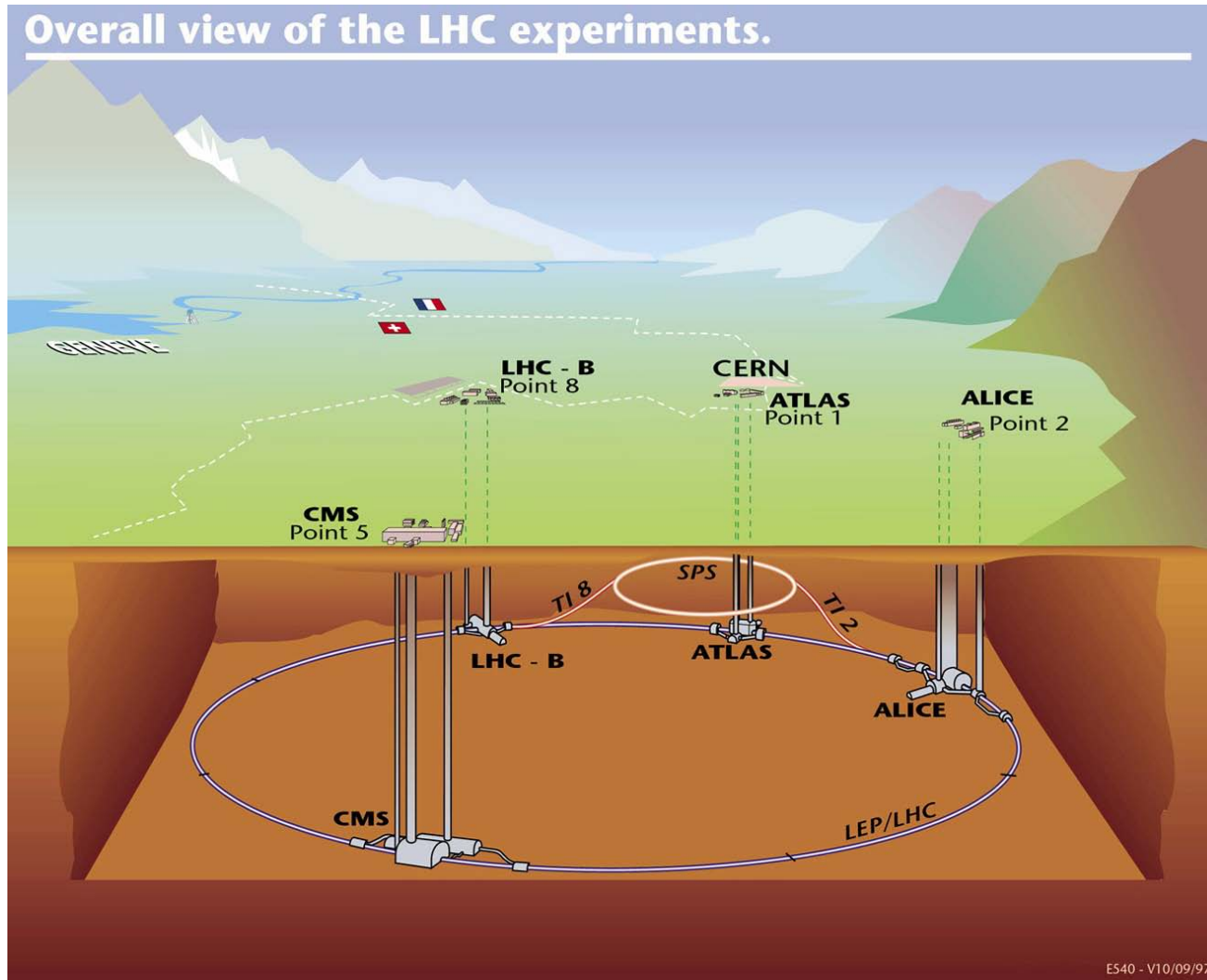
- Origin of mass
- Nature of Dark Matter
- Primordial Plasma
- Matter vs Antimatter

The LHC results will determine the future course of High Energy Physics

Cryodipole



CERN - Particle Accelerators



CERN - Particle Accelerators



LHC - Compact Muon Solenoid (CMS)



CMS Collaboration



36 Nations, 159 Institutions, 1940 Scientists (February 2003)

TRIGGER & DATA ACQUISITION

Austria, Finland, France, Greece, Hungary, Italy, Korea, Poland, Portugal, Switzerland, UK, USA

TRACKER

Austria, Belgium, Finland, France, Germany, Italy, Japan*, New Zealand, Switzerland, UK, USA

CRYSTAL ECAL

Belarus, China, Croatia, Cyprus, France, Italy, Japan*, Portugal, Russia, Serbia, Switzerland, UK, USA

PRESHOWER

Armenia, Belarus, Greece, India, Russia, Taipei, Uzbekistan

RETURN YOKE

Barrel: Czech Rep., Estonia, Germany, Greece, Russia
Endcap: Japan*, USA, Brazil

SUPERCONDUCTING MAGNET

All countries in CMS contribute to Magnet financing in particular:
Finland, France, Italy, Japan*, Korea, Switzerland, USA

FEET
Pakistan
China

FORWARD CALORIMETER

Hungary, Iran, Russia, Turkey, USA

HCAL

Barrel: Bulgaria, India, Spain*, USA
Endcap: Belarus, Bulgaria, Russia, Ukraine
HO: India

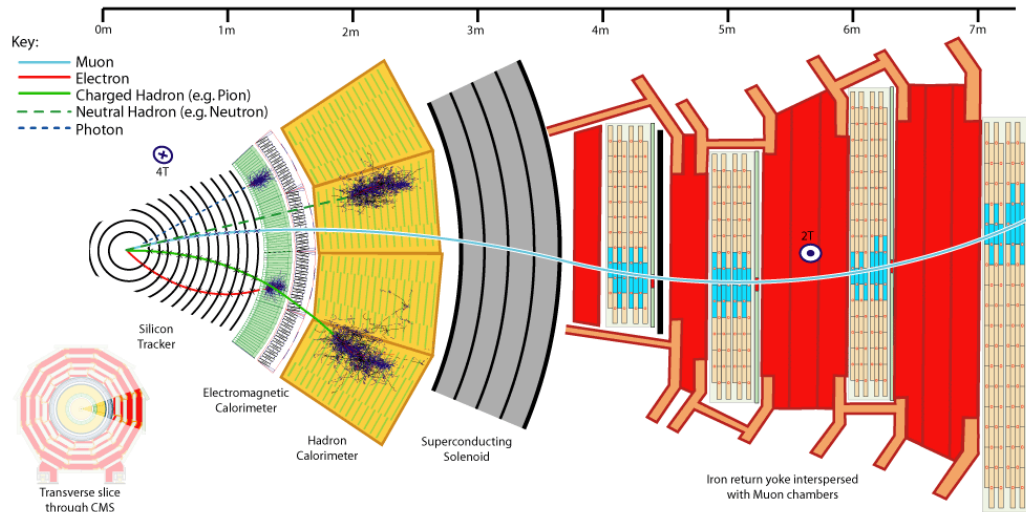
MUON CHAMBERS

Barrel: Austria, Bulgaria, China, Germany, Hungary, Italy, Spain,
Endcap: Belarus, Bulgaria, China, Korea, Pakistan, Russia, USA

* Only through industrial contracts

Total weight : 12500 T
Overall diameter : 15.0 m
Overall length : 21.5 m
Magnetic field : 4 Tesla

LHC - CMS



Solenoid:

- Length: 13 m
- Diameter: 5.9 m
- Superconducting coil (NbTi)
- Current: 20 kA
- Operating temperature: 4.4 K (- 269 C)
- Magnetic Field:
 - 4 Tesla
 - x 100 000 Earth field
 - Stored energy: 2.7 GJ

- Tracker: Silicon Pixel and Silicon Microstrip
 - Measurement of momentum of electrically charged particles
 - Reconstruction of vertices (interaction points + particle decays)
- Electromagnetic Calorimeter: Crystals of Lead Tungstate (PbWO4)
 - Measurement of the energy of: electrons/positrons and photons
- Endcap Preshower: Silicon Strip Sensors
 - Measurement of the transverse profile of electromagnetic showers
- Hadronic Calorimeter: Plastic Scintillators
 - Identification and measurement of quarks, gluons and neutrinos
 - Measurement of the energy and direction of jets
 - Measurement of missing transverse energy
- Muon chambers: Drift Tubes and Cathode Strip Chambers
 - Detection of muons

LHC - CMS

- Silicon Pixels
 - 150 μm x 100 μm
 - 66 million pixels
- Silicon Microstrips:
 - Sensor size: 11 cm x 16 cm (microstrip pitch 140 μm)
 - Total area: 214 m²
 - 11.4 million microstrips
- Electromagnetic Calorimeter
 - 22 to 23 cm long crystals
 - Avalanche Photodiodes (APDs) - barrel
 - Vacuum Phototriodes (VPTs) - endcaps
 - 76 000 detector elements (total)
- Endcap Preshower
 - Silicon strip sensors: 6.3 cm x 6.3 cm, 300 μm thick
 - 32 strips/sensor
 - 137 000 silicon strips

LHC - CMS

□ Hadronic Calorimeter

- 4 mm thick plastic scintillators
- Hybrid Photo-Diodes (external to the detector)
- 10 000 detector channels

□ Muon chambers

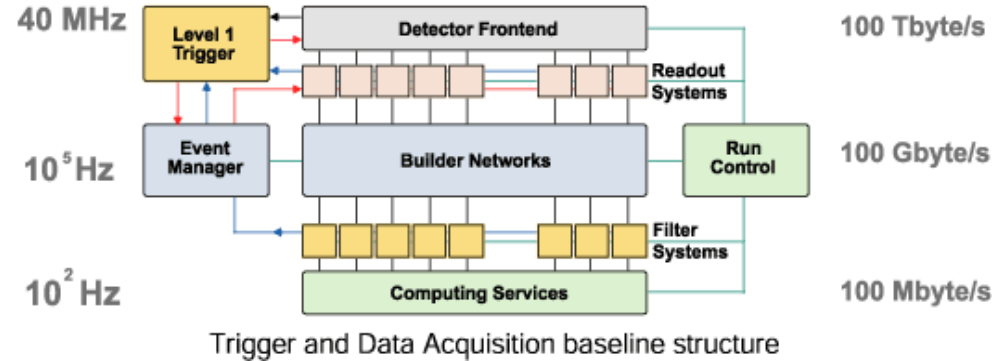
- Drift tubes (outside the solenoid)
- Cathode Strip Chambers (forward region)
- Resistive Plate Chambers
- 576 000 detector channels

Total number of detector channels ~78 million

CMS Trigger

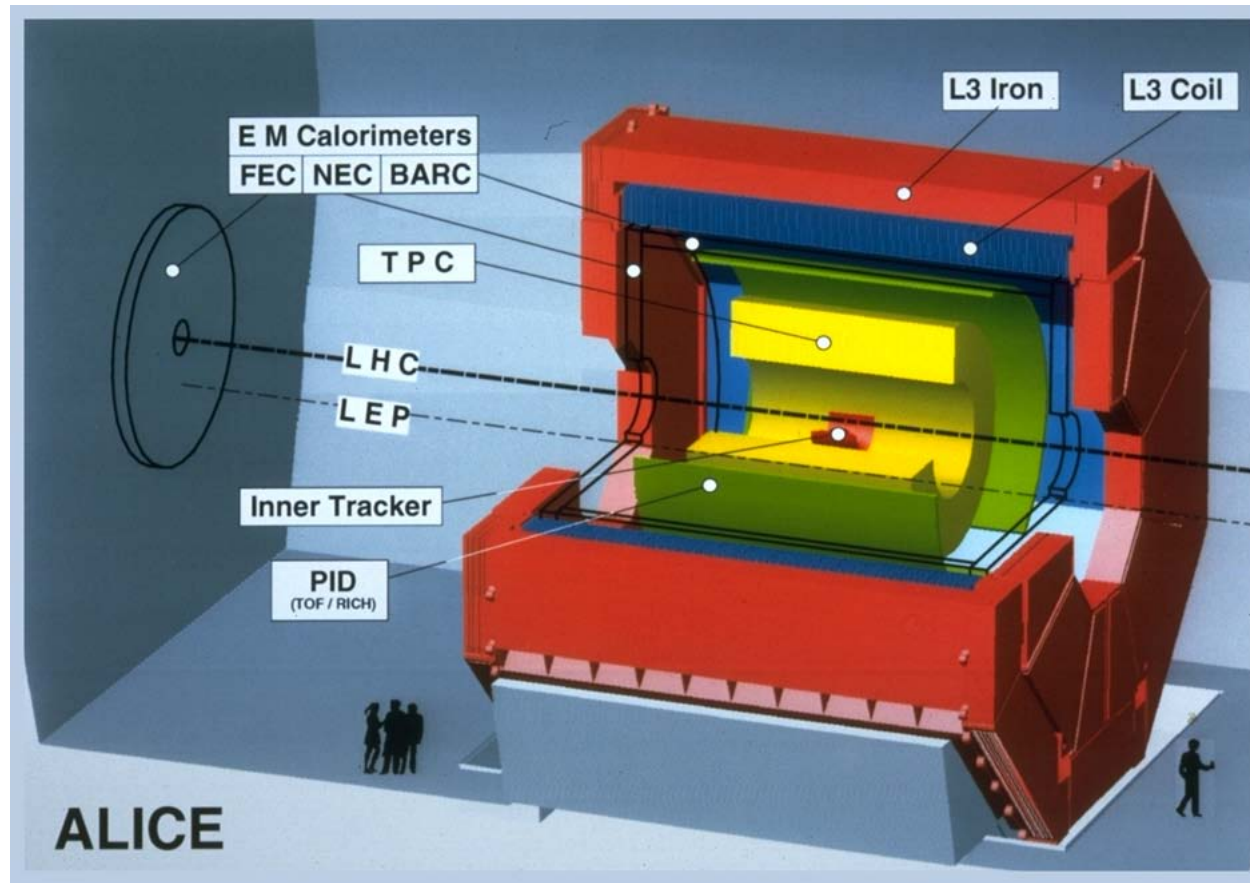
- Beam crosses: 40MHz/s
- 25 proton-proton collisions per beam crossing
- 78 M detector channels
- Brut force data collection would be the equivalent of 10 000 Encyclopaedia Britannica per second!
- Trigger system:
 - Identify the interesting events (about 100/s only)
 - Start the acquisition of interesting events
 - Only selected detectors contribute to the trigger (1 Mbyte event size)
- Trigger processing is done in three levels:
 - L1 custom hardware (100 kHz)
 - L2 commercial processors (100 Hz)
 - L3 uses full event data. Slow and Sophisticated analysis

Data Acquisition Main Parameters	
Collision rate	40 MHz
Level-1 Maximum trigger rate	100 kHz
Average event size	1 Mbyte
No. of electronics boards	10000
No. of readout crates	250
No. of In-Out units (200-5000 byte/event)	1000
Event builder (1000 port switch) bandwidth	1 Terabit/s
Event filter computing power	5 10^6 MIPS
Data production	Tbyte/day

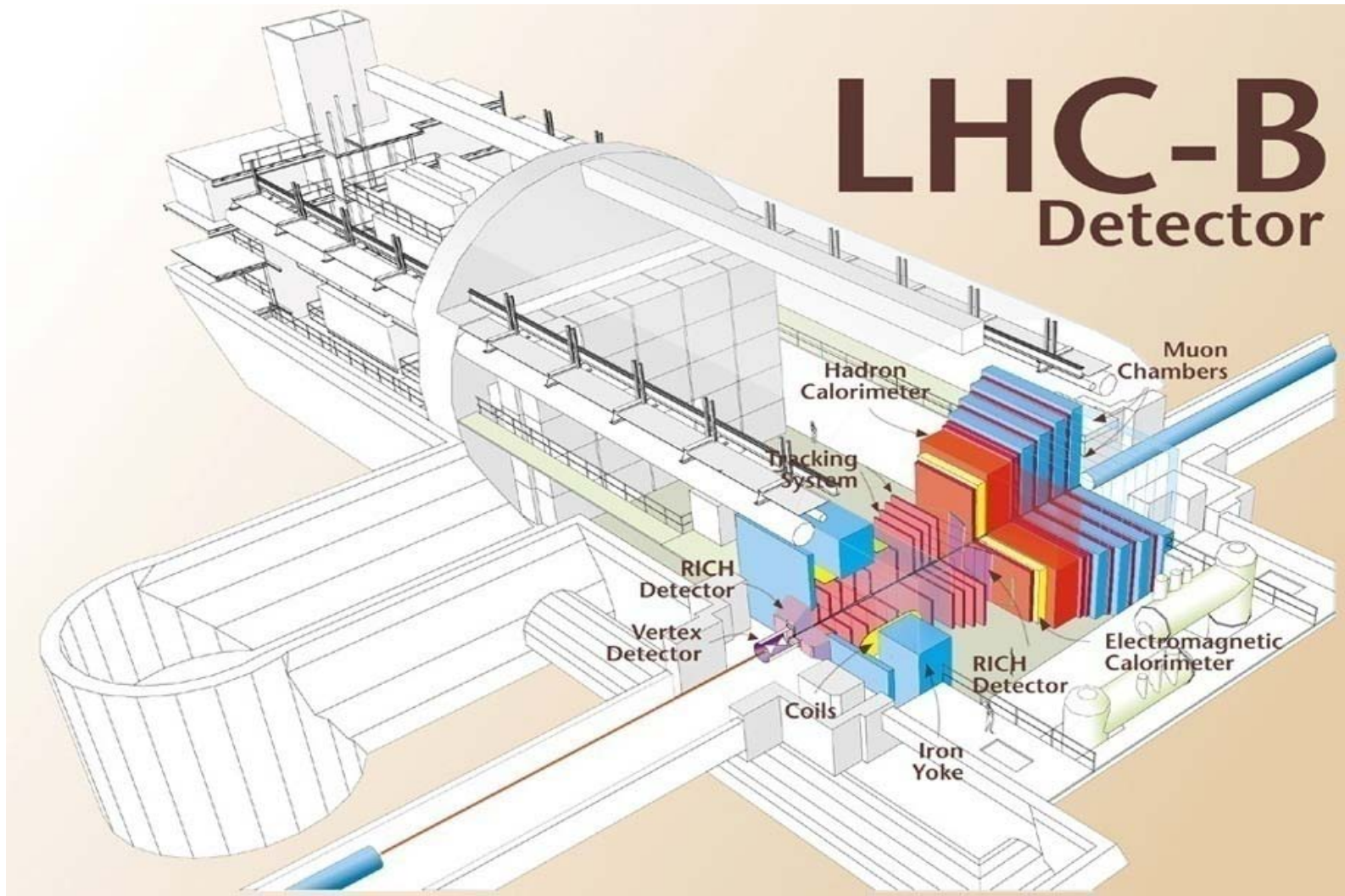


- Detector electronics contains memory to store the data to allow time for the trigger processor

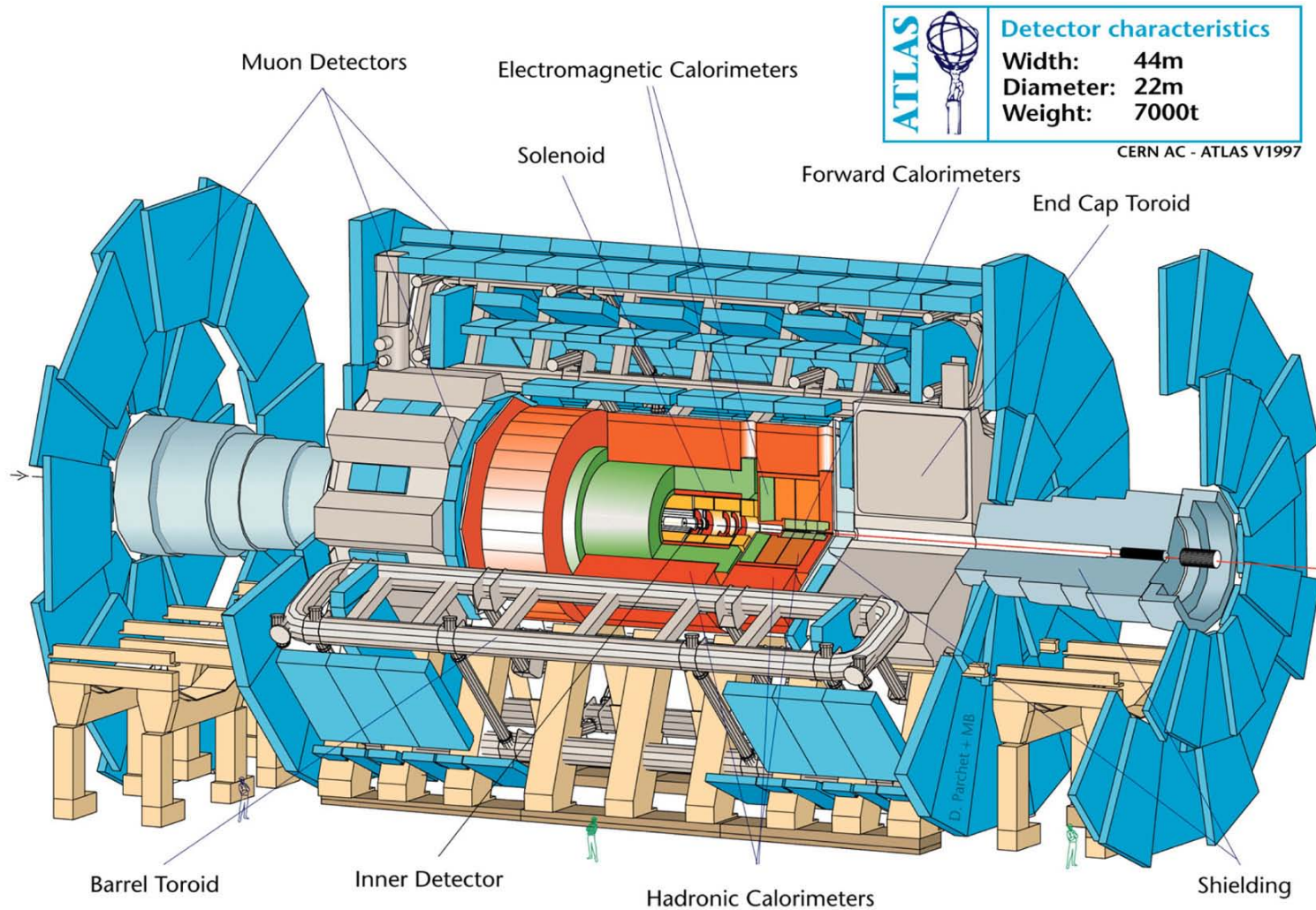
LHC - Particle Detectors: ALICE

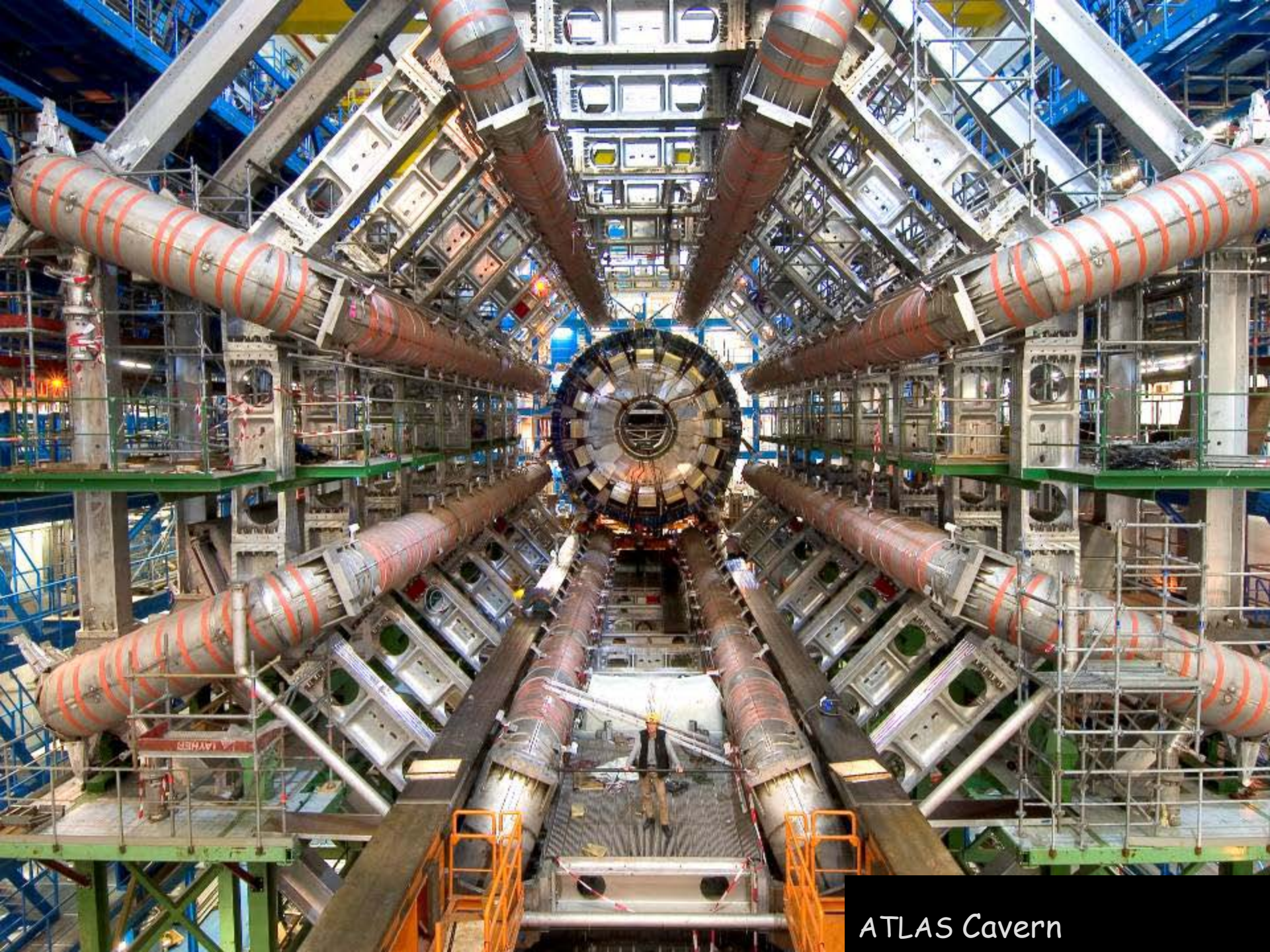


LHC - Particle Detectors: LHCb



LHC - Particle Detectors: ATLAS





ATLAS Cavern

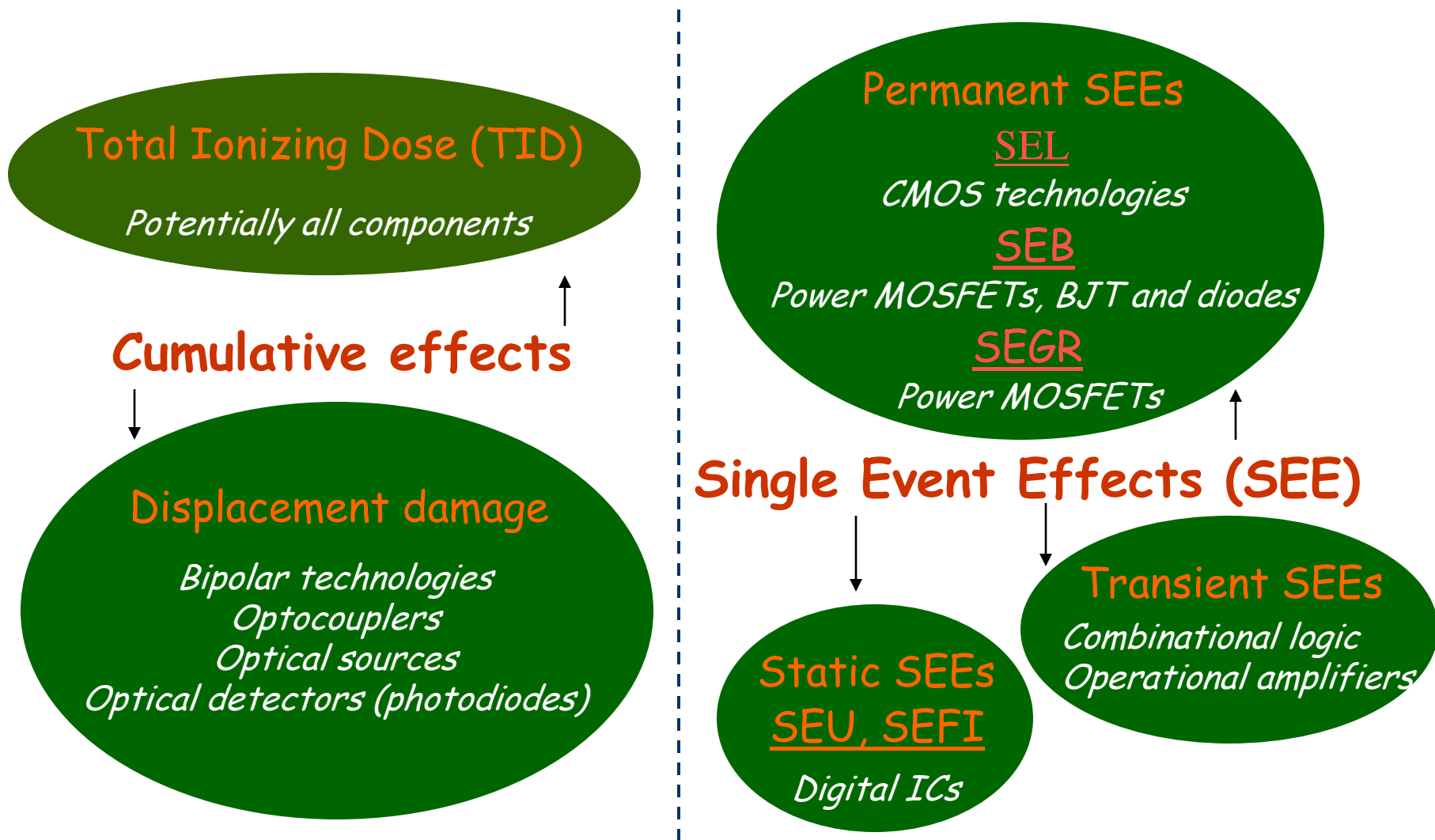
Radiation Levels in ATLAS:

During the experiment lifetime (10 years)

Detector zone	Total dose [rad]	Neutrons (1 MeV eq.) [n/cm ²]	Charged hadrons (> 21 MeV) [p/cm ²]
Pixels	112 M	$1.47 \cdot 10^{15}$	$2 \cdot 10^{15}$
SCT Barrel	7.9 M	$1.4 \cdot 10^{13}$	$1.1 \cdot 10^{14}$
ECAL (barrel)	5.1 k	$1.7 \cdot 10^{12}$	$3.6 \cdot 10^{11}$
HCAL	458	$2.5 \cdot 10^{11}$	$5.6 \cdot 10^{10}$
Muon detector	24.3 k	$3.8 \cdot 10^{12}$	$8.7 \cdot 10^{11}$

Satellite applications typical requirement: < 100 Krad

Summary of Radiation Effects



Total Ionizing Dose (TID)

Ionization in SiO_2
In LHC: (charged hadrons,
electrons, gammas, neutrons)



Creation of electron-hole pairs



Buildup of charge/defects



Device degradation

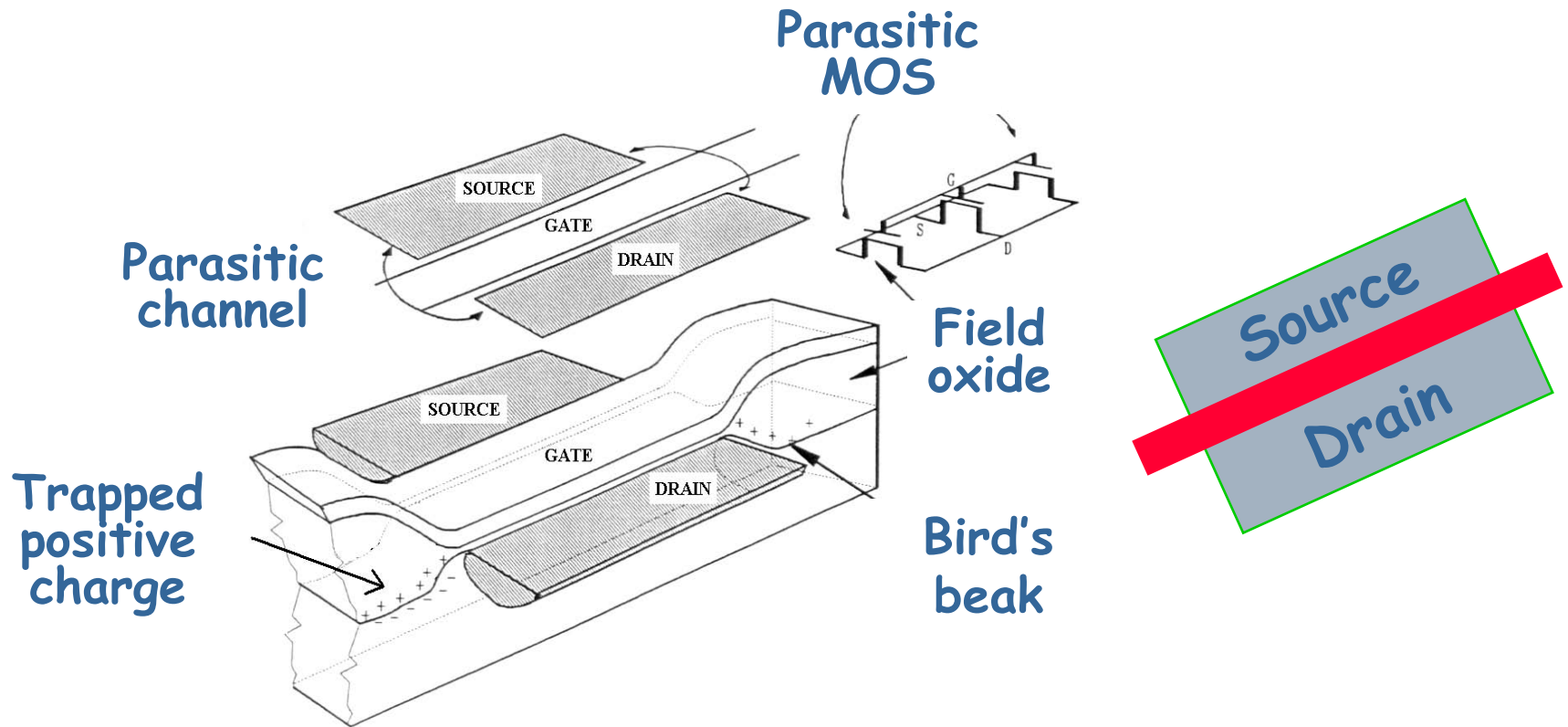
Trapped holes:

- Vt shift
- Noise
- Leakage
- Fast formation
- Annealing

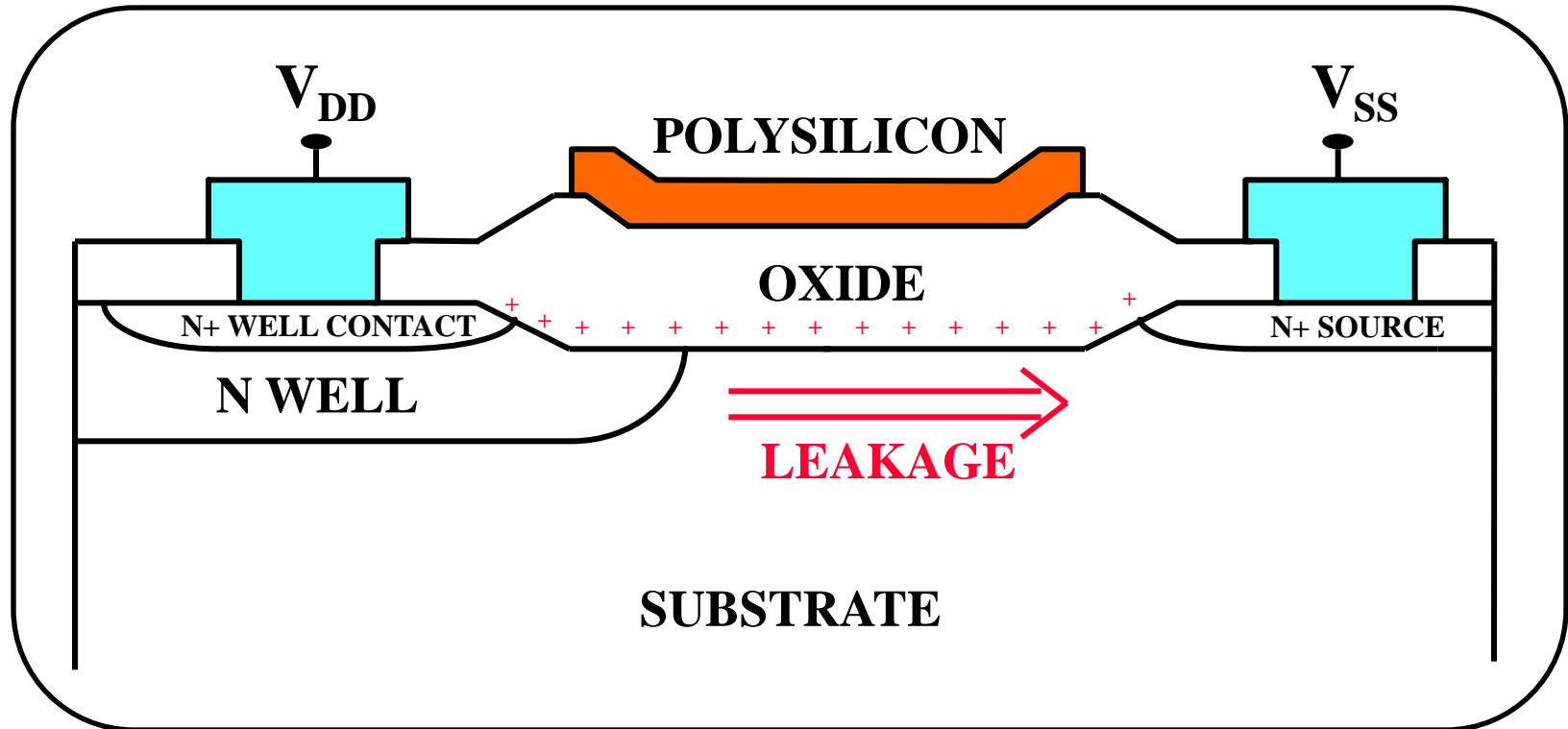
Interface States:

- Vt shift
- Mobility
- Transconductance
- Slow formation
- No annealing < 400 C

Transistor Level Leakage



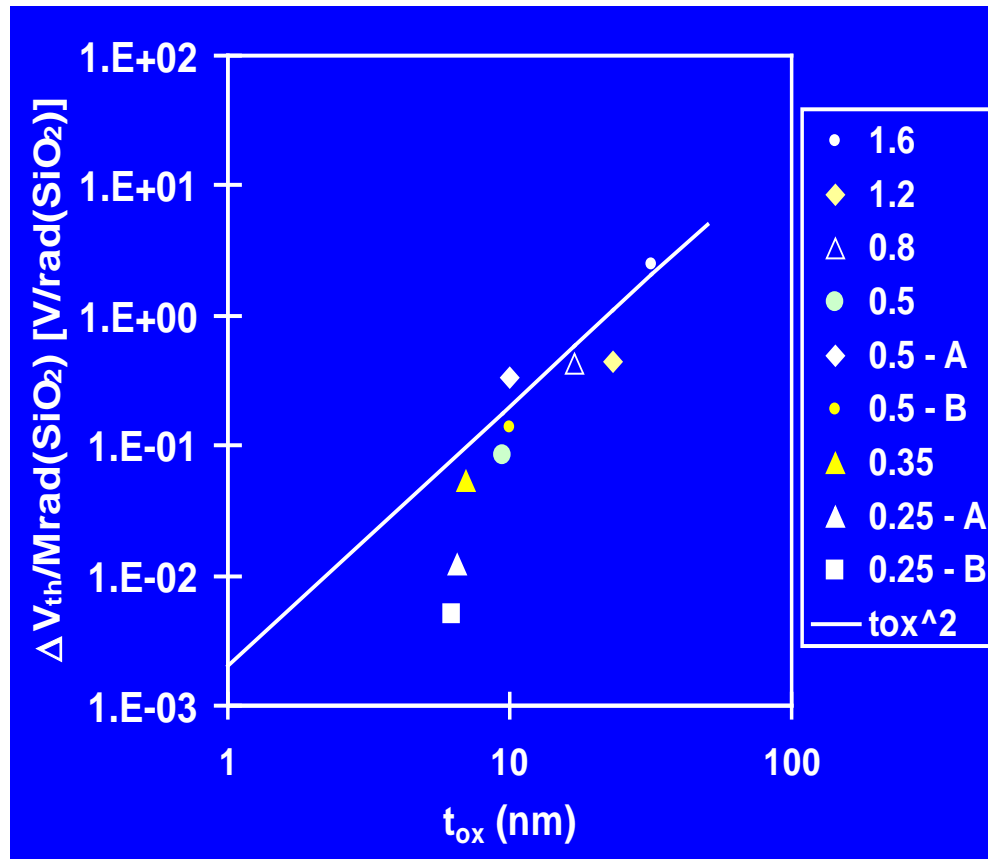
IC Level Leakage



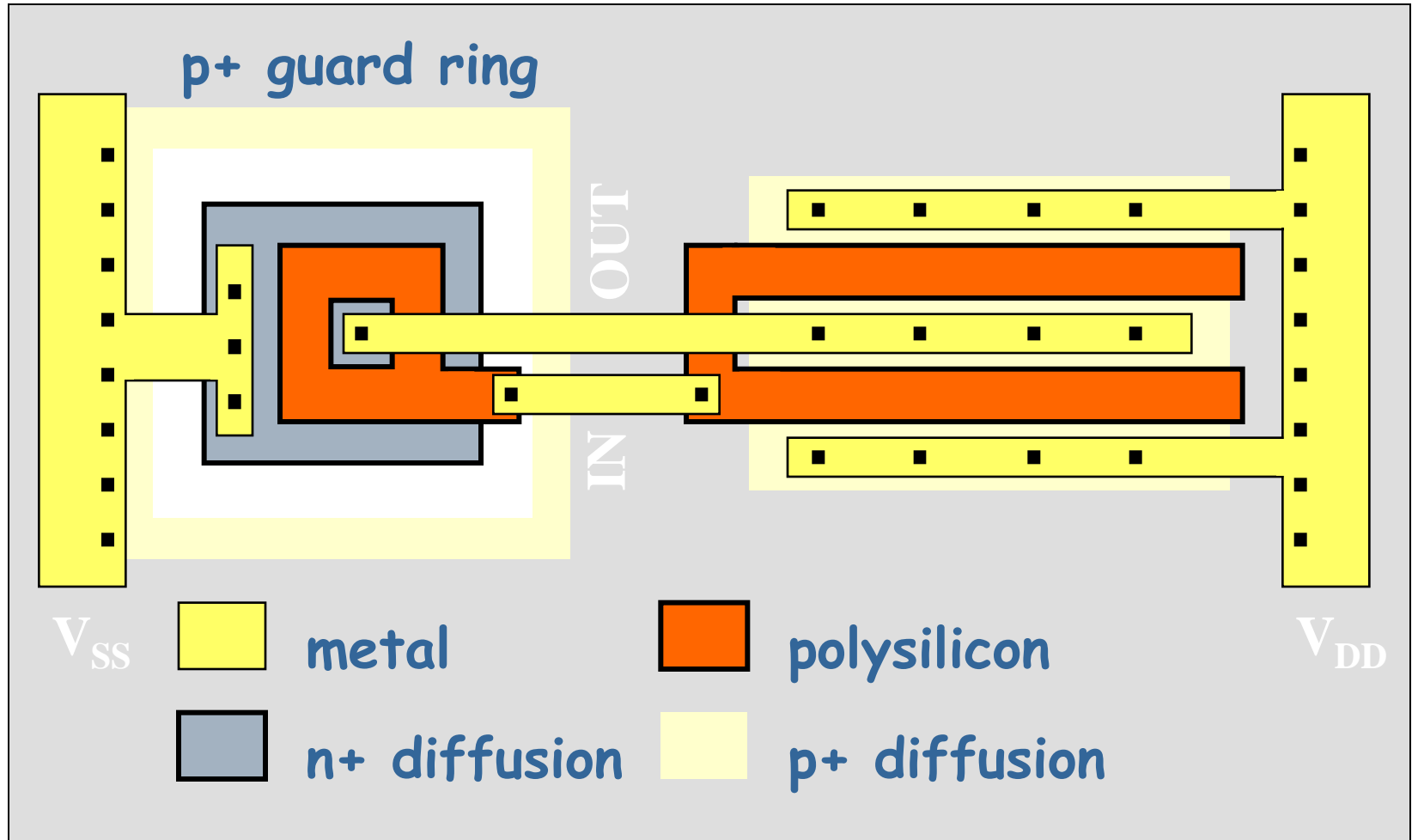
Radiation Effects and t_{ox} Scaling

Damage decreases with gate oxide thickness

Measured on VLSI tech.



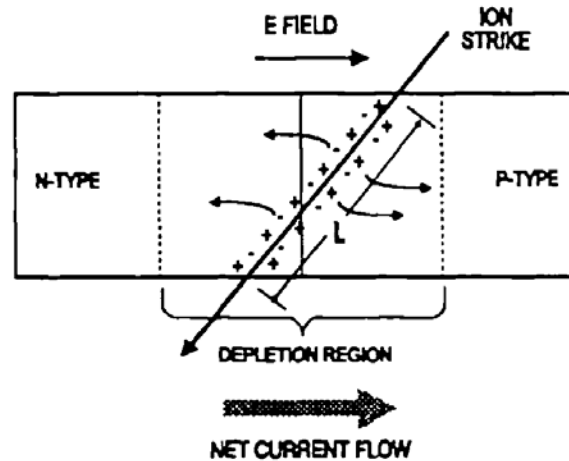
Radiation Tolerant Layout Approach



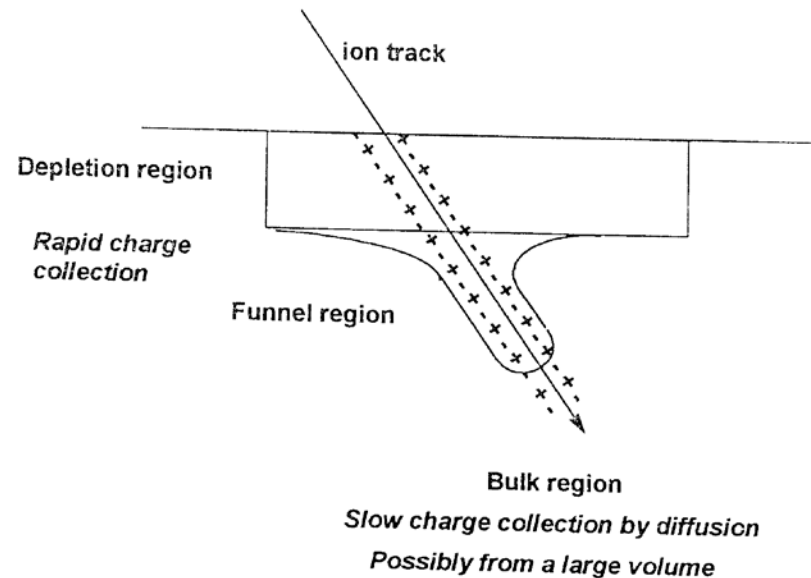
Single Event Upset (SEU)

Along the ion track, e-h pairs are created. In presence of an electric field (depleted junction), the charge will flow and a current spike might be observed.

Charge collection has a prompt and a slow component, and might extend far from the depleted junction (funneling)

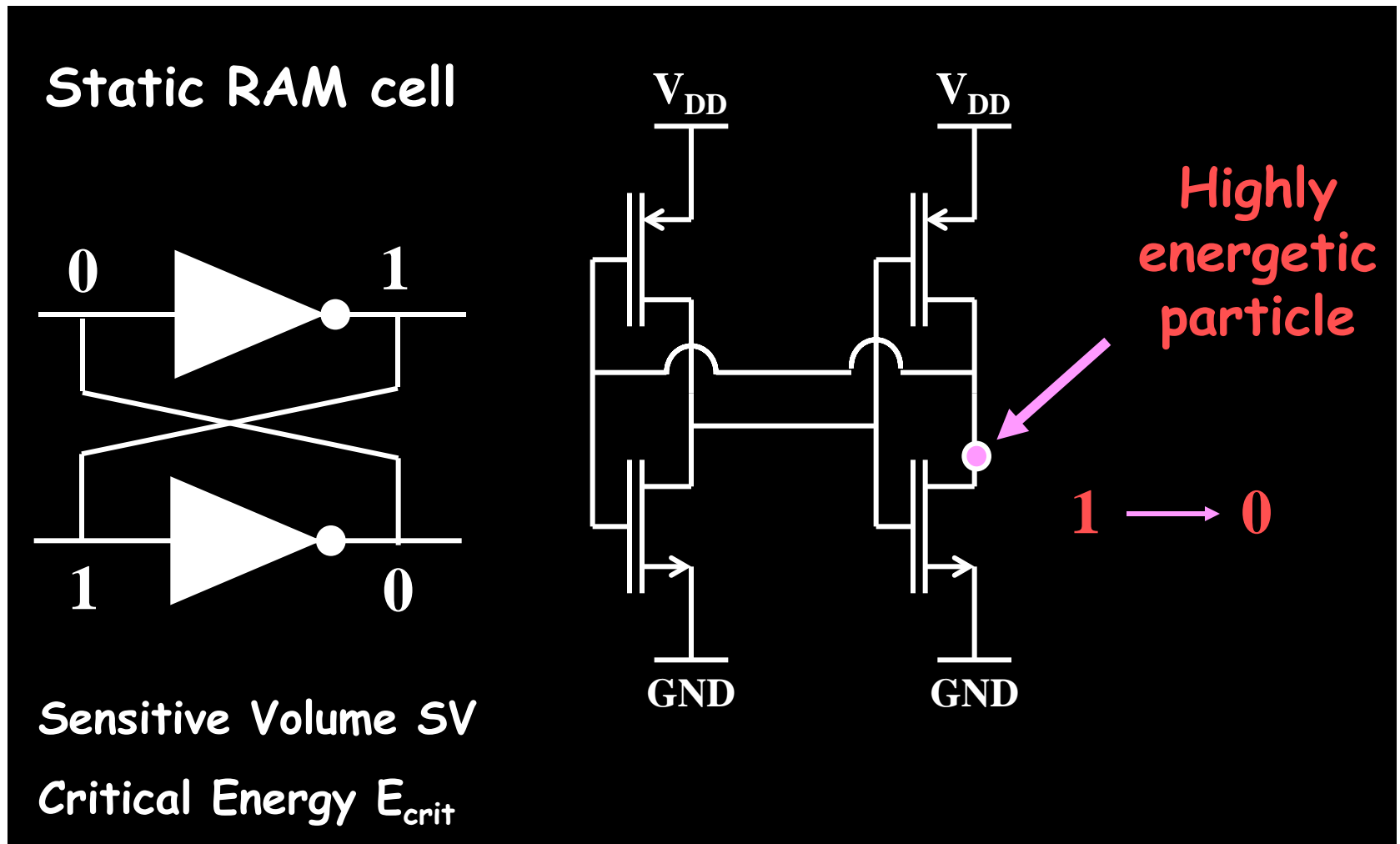


L.Massengill,
IEEE NSREC
short course,
1993



E.L.Petersen,
IEEE NSREC
short course,
1997

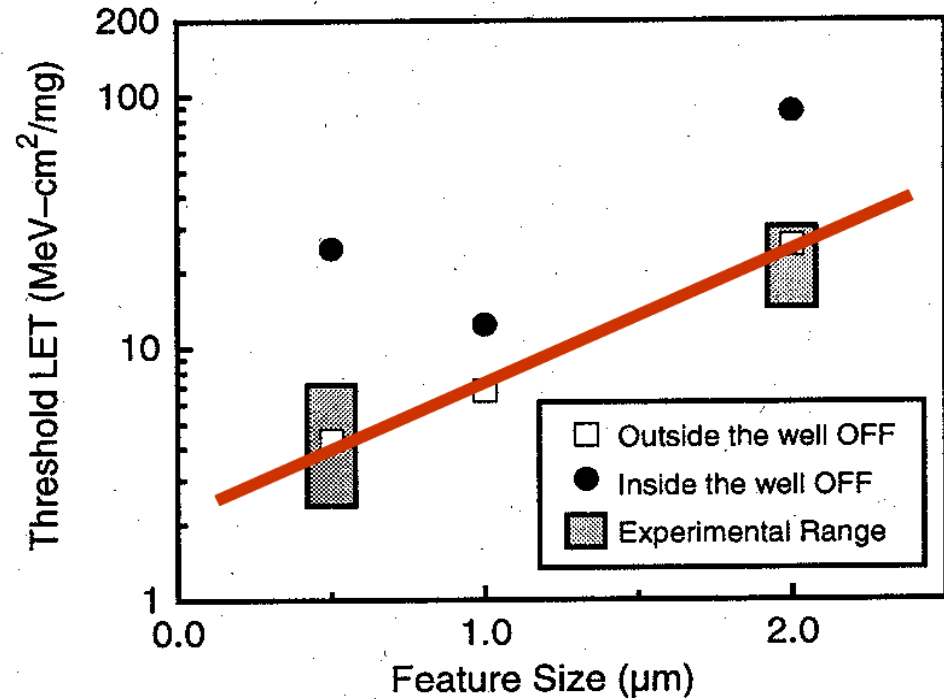
Single Event Upset (SEU)



SEU and Scaling

The SEU problem worsens with scaling

- V_{DD} reduced
- Node C reduced

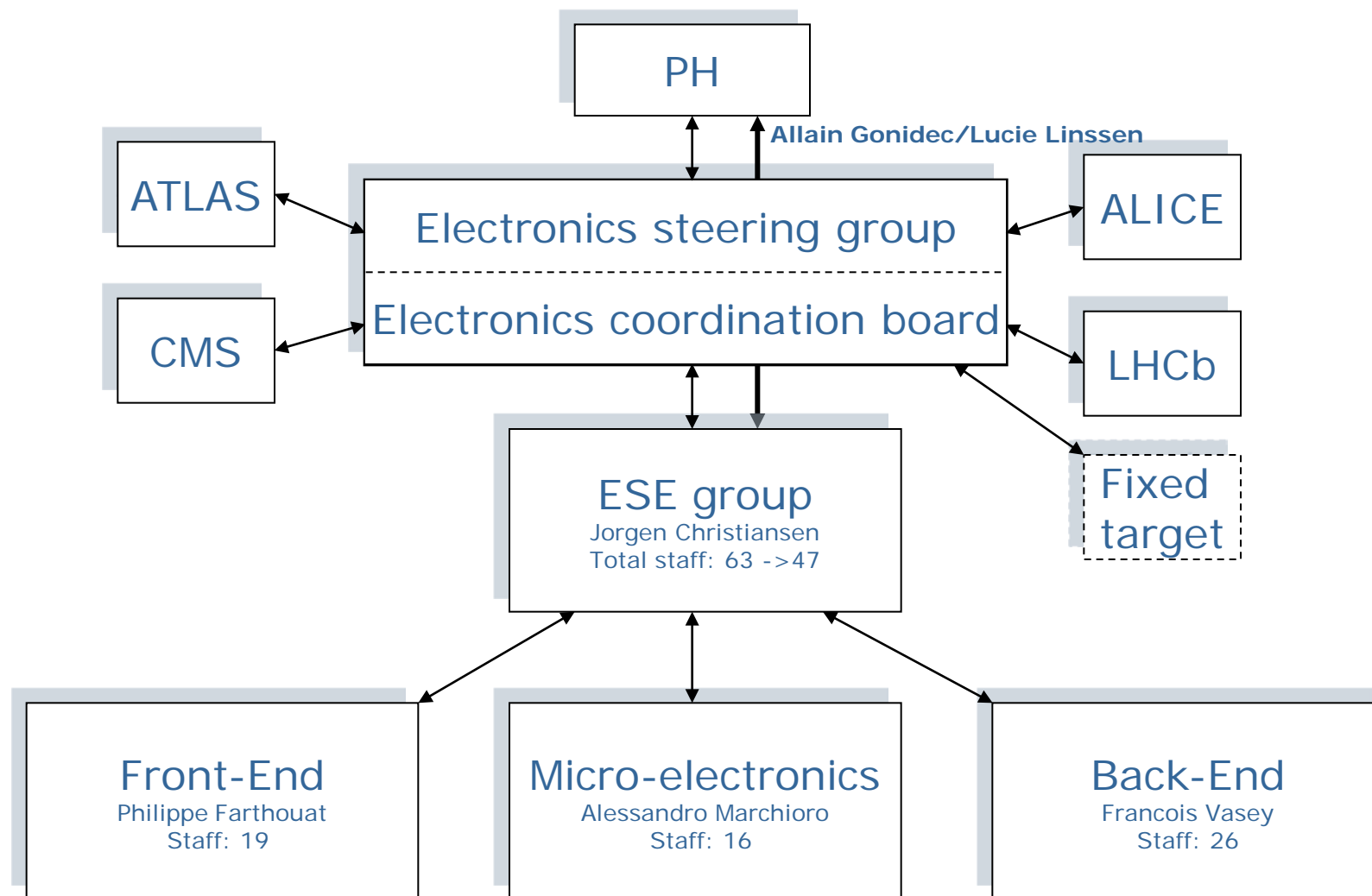


P.E. Dodd et al., IEEE TNS, Dec. 1996

SEU Robustness

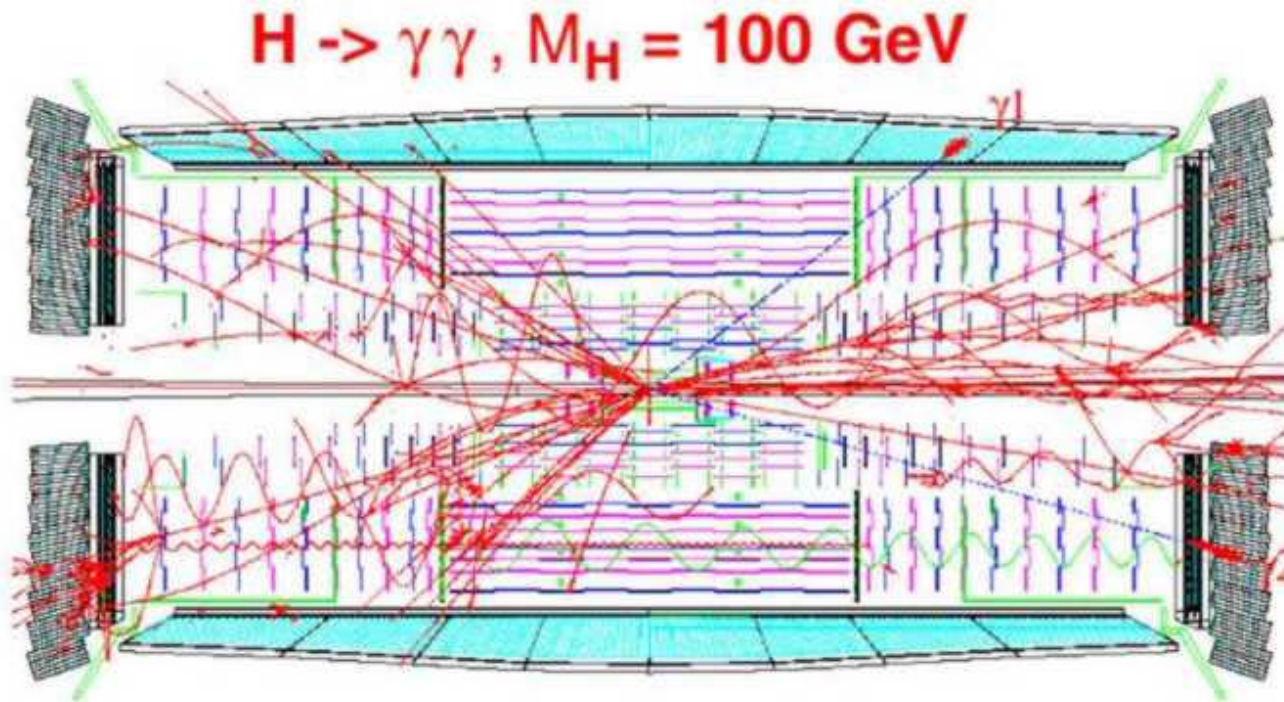
- ❑ Technology level (epitaxial substrates, SOI,...)
- ❑ Cell design (SEU-tolerant FF or memories)
- ❑ Voting (block or system level)
- ❑ EDAC techniques (system level)
- ❑ Duplication of the information (example: configuration data for FPGA)
- ❑ Special "error immune" architecture
- ❑ Always to be considered at system level

Electronics Systems for Experiments (ESE - 2008)



The Timing Trigger and Control (TTC) system

- The electronics inside/outside the detector has to work synchronously with the accelerator clock:
- Electronics synchronization is done at two levels:
 - Clock synchronization
 - Event tagging



The TTC system

□ Clock Synchronization

- Multiple collisions will occur at a rate of **25 ns**
- The electronics will run at this frequency **40 MHz**
- Some detectors (or parts of them) require the clock phases to be within a **few hundreds of ps**
- Clock jitter **< 50 ps** for some systems
- This function can be compared to a clock tree network in and ASIC:
 - This has to be made all over the detector volume
 - 7600 m³ for CMS
 - 33400 m³ for ATLAS
- The system has to compensate for:
 - Intrinsic delays in the electronics
 - Signal distribution delays in cables/optical fibres
 - Travel times of the particles inside the detectors

The TTC system

- Event tagging:
 - All the “collisions” must be marked with the collision number (Bunch Crossing Number)
 - Once an interesting physics phenomena is detected (called an event) data has to be marked with an Event Number.
- Data is transmitted out of the detectors:
 - Synchronously:
 - Triggers systems: finding events
 - Only a fraction of the detector’s data
 - BCN used to check data alignment
 - Asynchronously:
 - Event data can be transmitted asynchronously
 - BCN and EN are used for event reconstruction

The TTC receiver ASIC (TTCrx)

□ Functionality:

- Clock Deskewing
- Tagging
- Slow control commands

□ It is the end element of an optical distribution network:

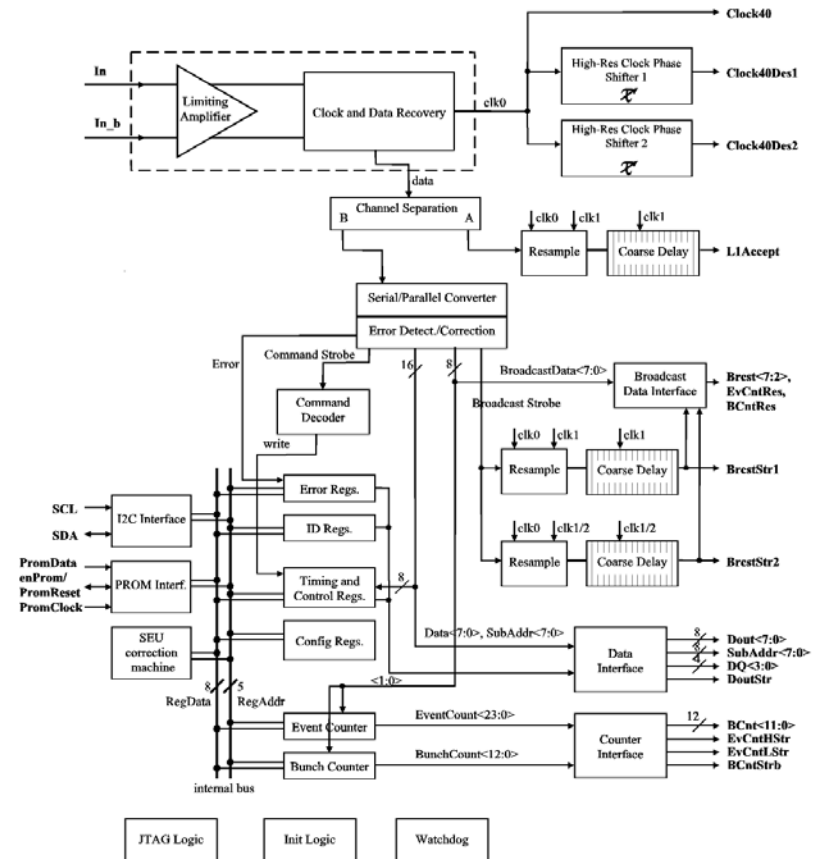
- Single laser source
- Two time division multiplexed channels 80 Mbit/s
- Up to 1024 destinations

□ Functions:

- "Optical" post-amplifier
- Deserializer
- TD demultiplexer
- Clock recovery PLL
- 4 Clock de-skewing DLLs'

□ Radiation Tolerance:

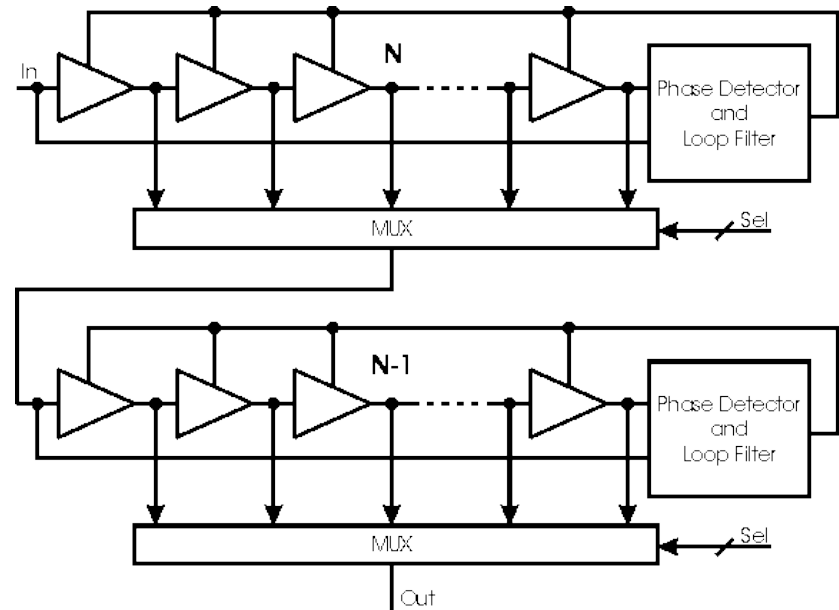
- Hardened technology: 0.8 μ m DMILL
- Registers Hamming encoded
- Critical registers duplicated



TTCrx: Clock Deskewing

- Implementation:
 - 1 μm CMOS (0.8 μm final)
 - Required resolution less than a buffer delay
- A “Vernier” method was adopted to achieve the required resolution
 - Two Delay-Locked Loops (DLL) are used in series
 - One divides the reference clock period in N equal intervals while the other one in $N-1$
 - The multiplexers “program” the clock phase
 - Since the clock is a periodic signal the “apparent” time resolution is:

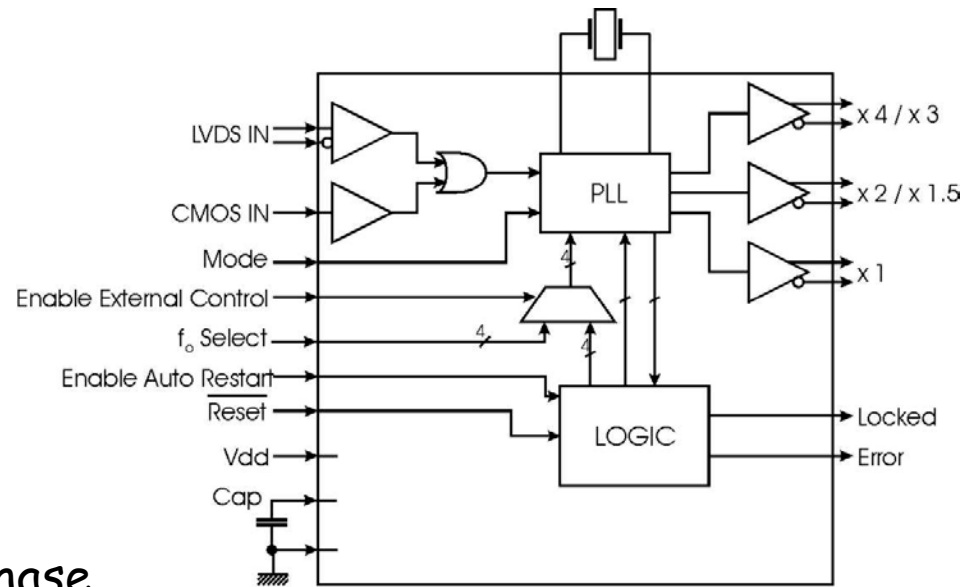
$$\Delta t = \frac{1}{N \cdot (N - 1)} \times T$$



- Circuit parameters:
 - $T = 25 \text{ ns}$
 - $N = 16$
- Resolution:
 - $\Delta t = 104 \text{ ps}$
 - $\sigma(\text{diff}) = 48 \text{ ps}$
 - $\text{pp}(\text{diff}) = 324 \text{ ps}$
 - $\sigma(\text{int}) = 74 \text{ ps}$
 - $\text{pp}(\text{int}) = 326 \text{ ps}$

QPLL:

- TTC system jitter excessive for:
 - Gbit/s Serializers and Deserializers
 - High resolution TDCs
 - High resolution ADCs
- QPLL: a PLL based on a VCXO:
 - VCXO - intrinsic low phase noise
 - Ideal for narrow band PLLs
 - Ideal for jitter filtering
- LHC nominal frequency:
 - 40.078666 MHz \pm 12 ppm



QPLL: Operation Principles

□ Phase detector:

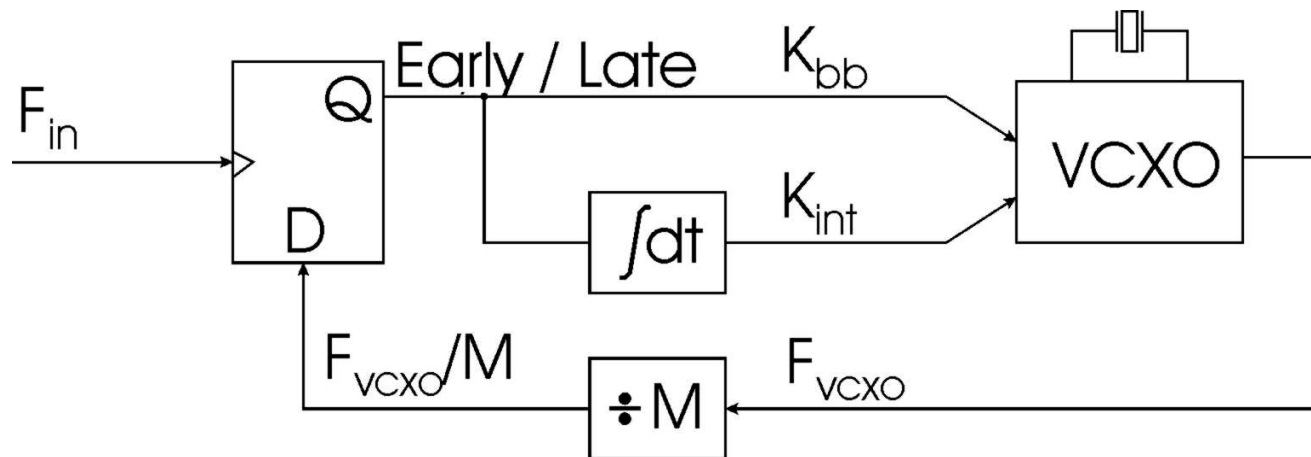
- Bang-bang type
- Only early/late decision

□ VCXO

- Two control ports
- Bang-bang control
- Continuous control

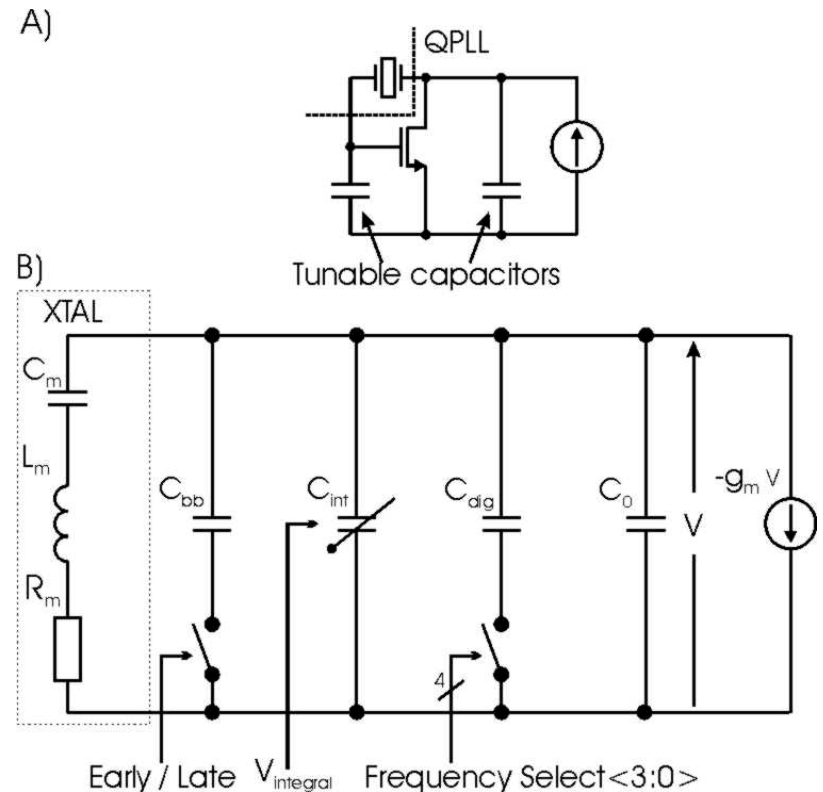
□ Control loop:

- Two control branches
- Bang-bang: phase and frequency control
- Integral: average frequency control
- Almost independent optimization of K_{bb} and K_{int}



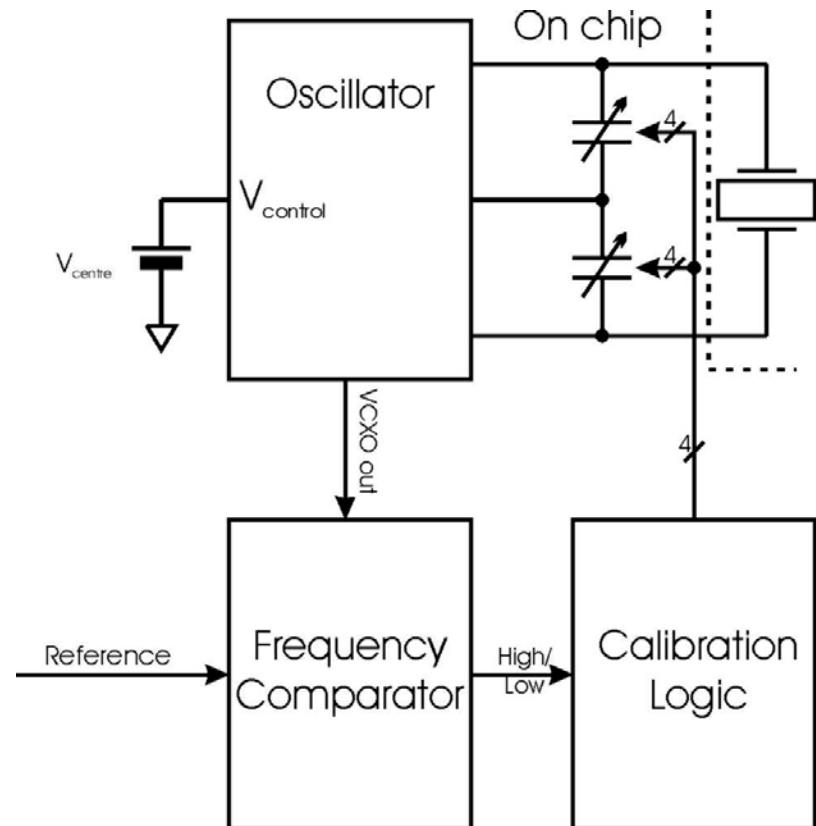
QPLL: Operation Principles

- VCXO:
 - Pierce Oscillator
 - Two frequency control capacitors
- Three frequency control mechanisms:
 - Bang-bang control:
 - switched capacitor
 - Integral control:
 - voltage controlled n-well capacitor
 - Frequency centering:
 - four binary weighted switched capacitors. (Not under the PLL loop control)



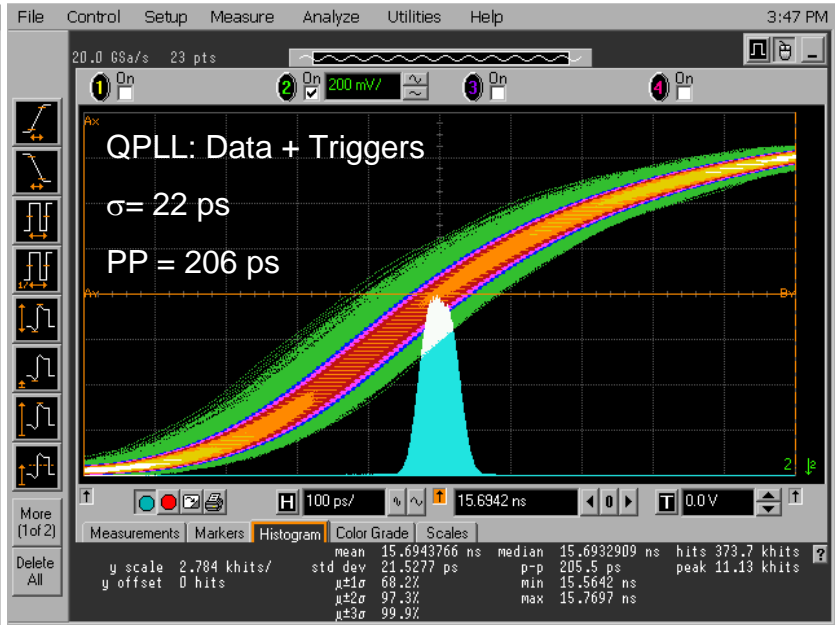
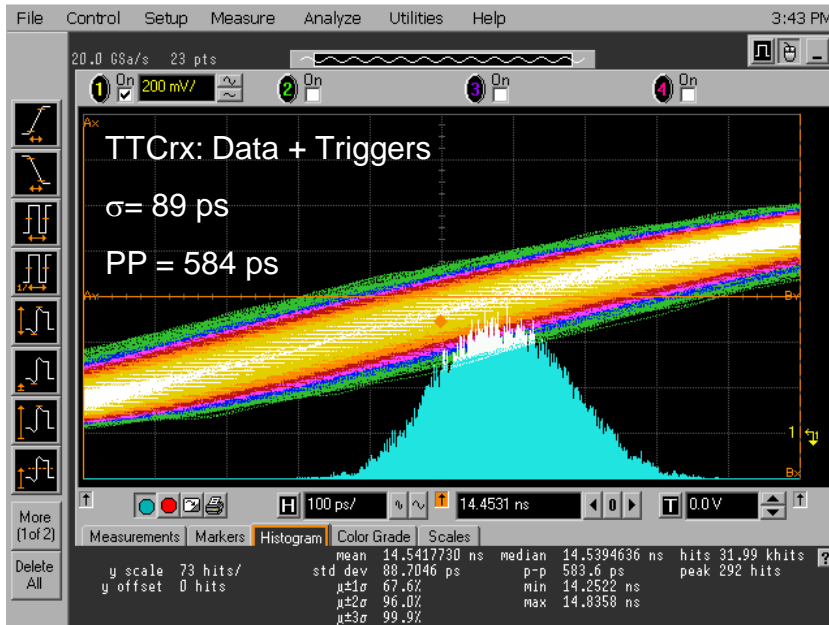
QPLL: Operation

- Lock acquisition, two phases:
 - Frequency centering
 - Standard frequency pull-in and phase lock cycle
- Frequency centering:
 - After start-up, reset or unlocked operation detected
 - Frequency-only detector used
- Frequency centering operations:
 - The bang-bang loop is disabled
 - The VCXO control voltage forced to its mid range value
 - A binary search is made to decide on the value of the frequency centering capacitor
 - Once the value found, control is passed to the PLL control loop



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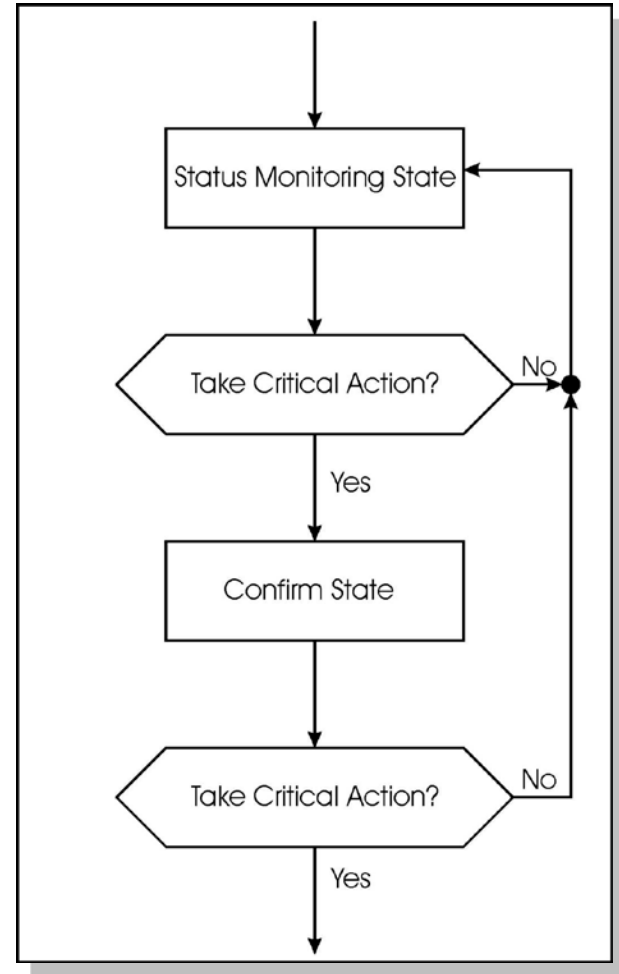


54855A Infinium Oscilloscope

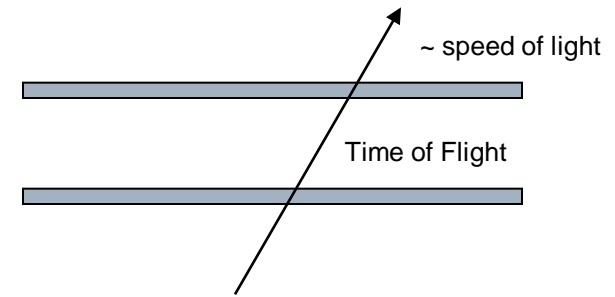
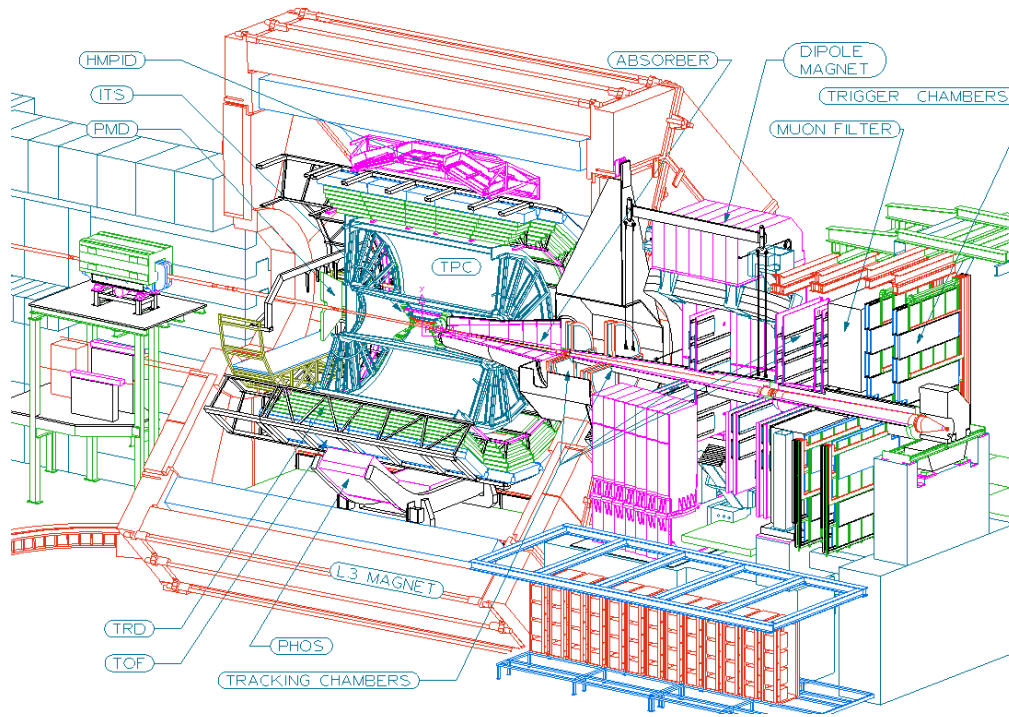
- Analog bandwidth: 6 GHz
- Real-time sampling
- Sample rate: 20 GSa/s

QPLL: Radiation Tolerance

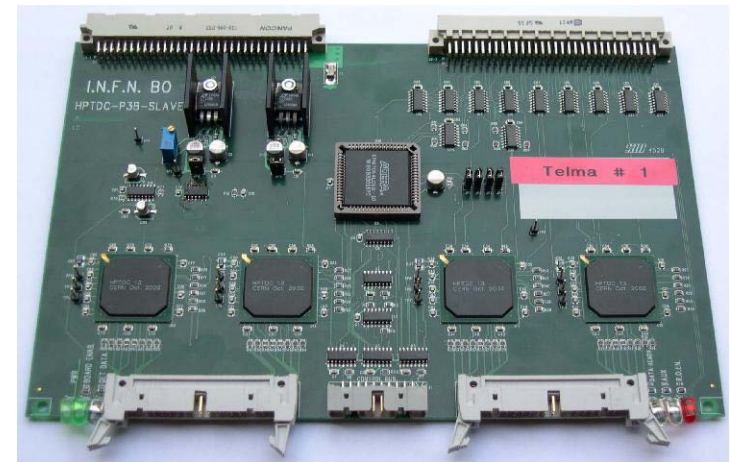
- Total dose:
 - 0.25 μm CMOS process
 - Enclosed NMOS
 - Guard rings
- Single Event Upsets:
 - Majority voting circuits
 - Confirm before acting
 - When in doubt, take the action with less impact for the system



ALICE Time Of Flight (TOF) Detector

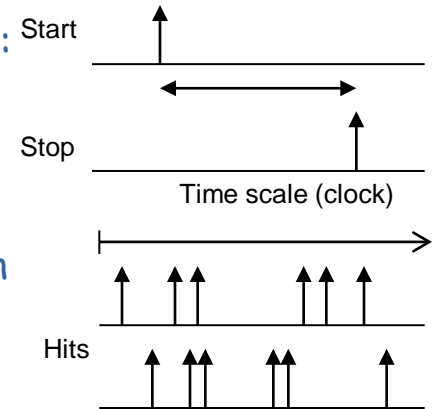


- ~25 ps resolution
- 160.000 channels
- Low hit rate: few tens of kHz
- Trigger rate: few kHz
- Trigger latency: 6.7 us
- Trigger window: 100ns



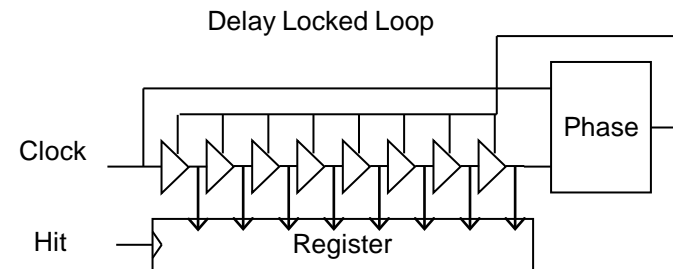
What is a TDC and its use

- TDC's are used to measure time (intervals) with high precision
 - Start - stop measurement
 - Measurement of time interval between two events:
 - start signal - stop signal
 - Used to measure relatively short time intervals with high precision
 - Time tagging
 - Measure time of occurrence of events with a given time reference:
 - Time reference (Clock) - Events to be measured (Hit)
 - Used to measure relative occurrence of many events on a defined time scale
- Special needs for high energy physics
 - Many thousands of channels needed
 - Rate of measurements can be very high
 - Very high resolution
 - A mechanism to store measurements during a given interval and extract only those related to an interesting event, signaled by a trigger, must be integrated with TDC function

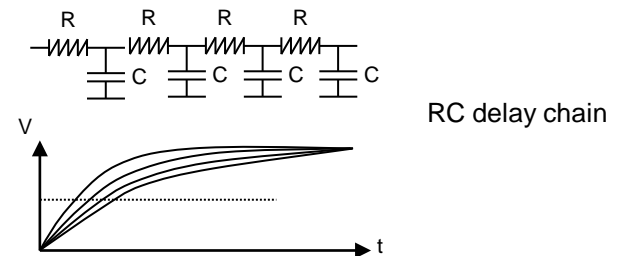


HPTDC: Operation principles

- Delay locked loop
 - Self calibrating using external frequency reference (clock)
 - Allows combination with counter
 - Delicate feedback loop design (jitter)

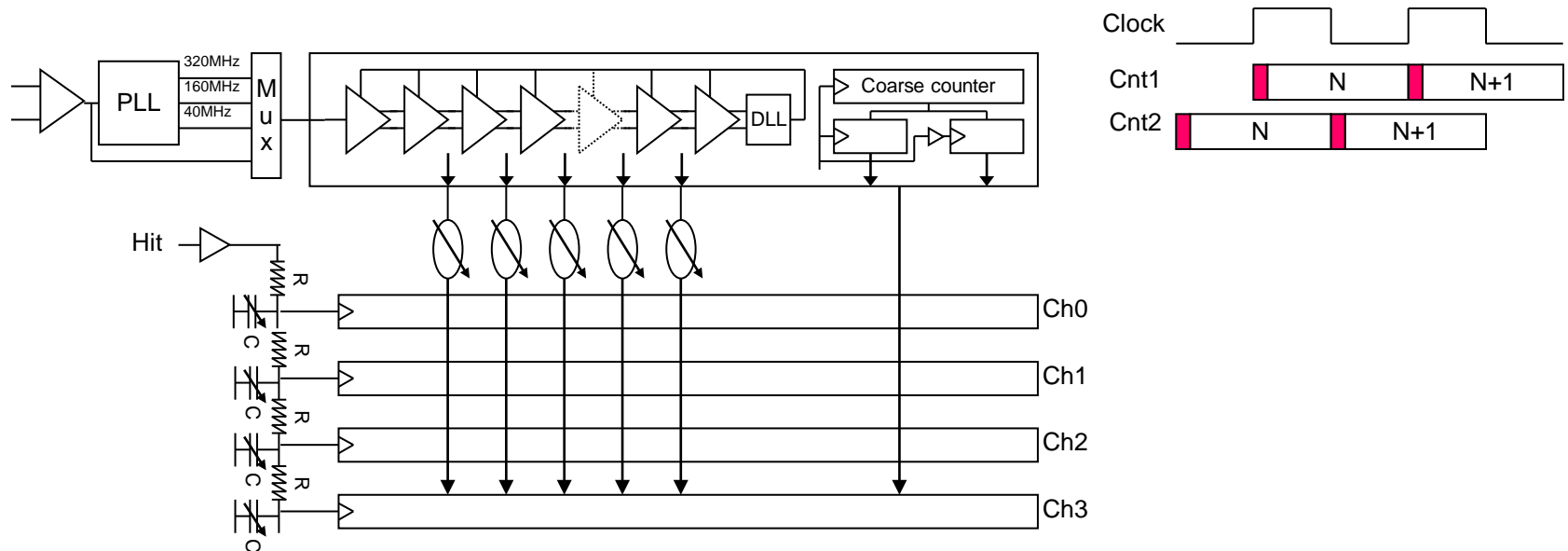


- R-C delay chain
 - Very good resolution
 - Signal slew rate deteriorates.
 - Delay chain with losses so only short delay chain possible
 - Large sensitivity to process parameters (and temperature)



HPTDC: Operation principles

- Combination of
 - Counter with PLL for clock multiplication (x1, x4, x8)
 - Double phase shifted counters to resolve possible metastability in coarse count measurement.
 - DLL with 32 taps for clock interpolation
 - Use of differential delay cell for power supply noise immunity
 - R-C delay line on hit signals for very high resolution
 - Channel reduction by factor 4 (8 channels per chip)

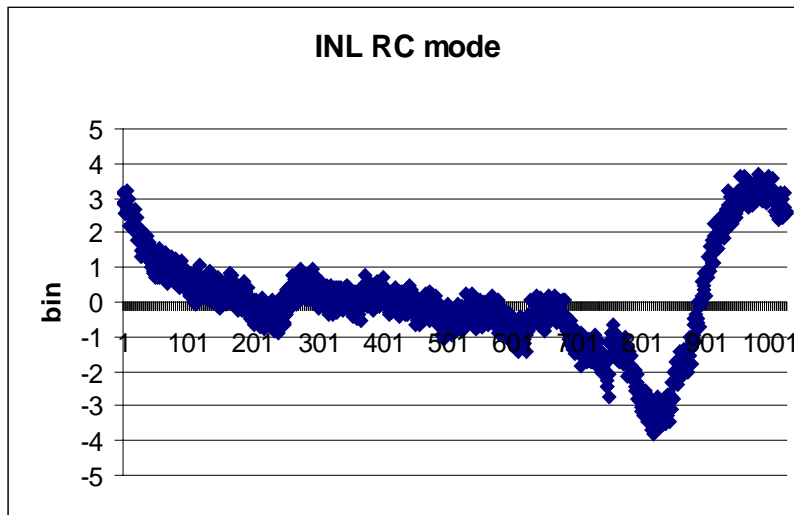
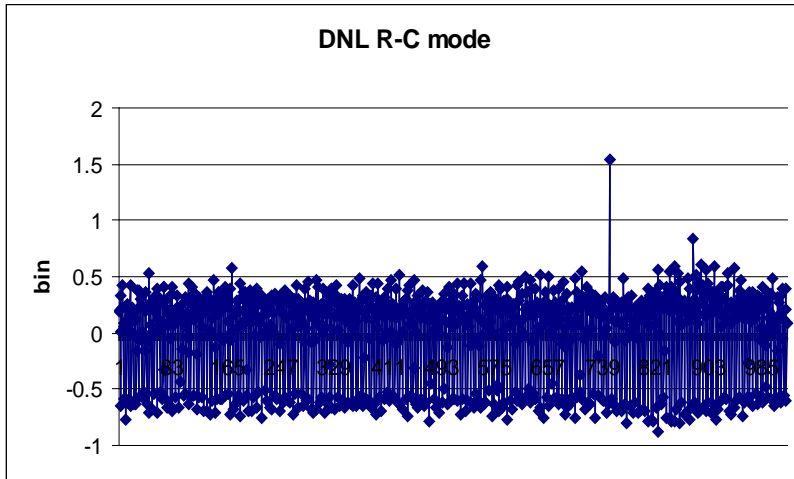


HPTDC: Operation principles

□ Very high resolution:

- R-C delay line dependent on IC processing (Only small difference between chips seen)
- R-C delay line independent of temperature in range of 20 deg
- Infrequent calibration required
- Calibration can be obtained with code density test with physics hits
- Option of correcting integral errors from DLL
- 8 channels per chip
- Not possible to pair leading and trailing edges

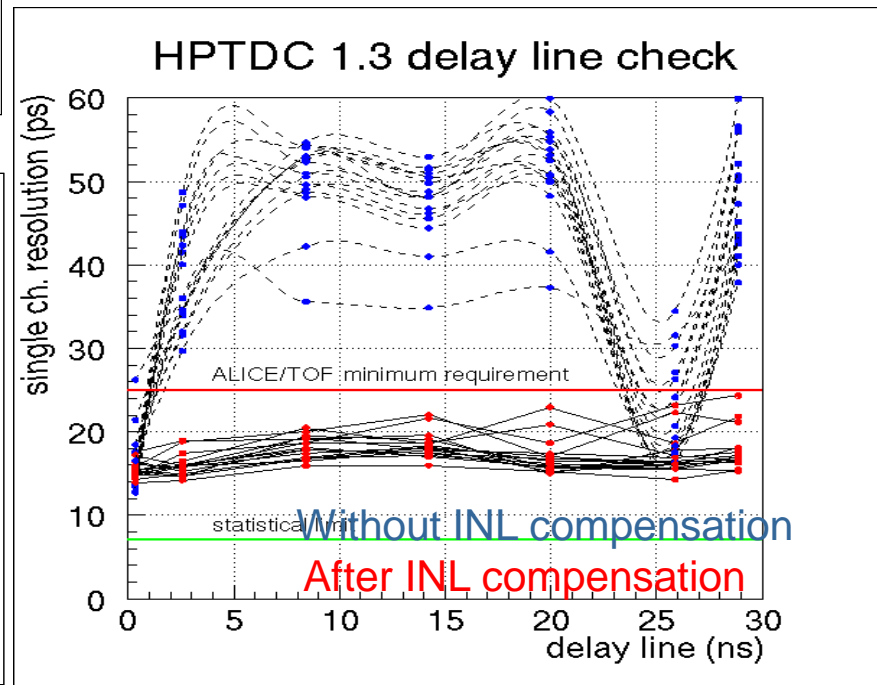
HPTDC: Very high resolution (R-C mode)



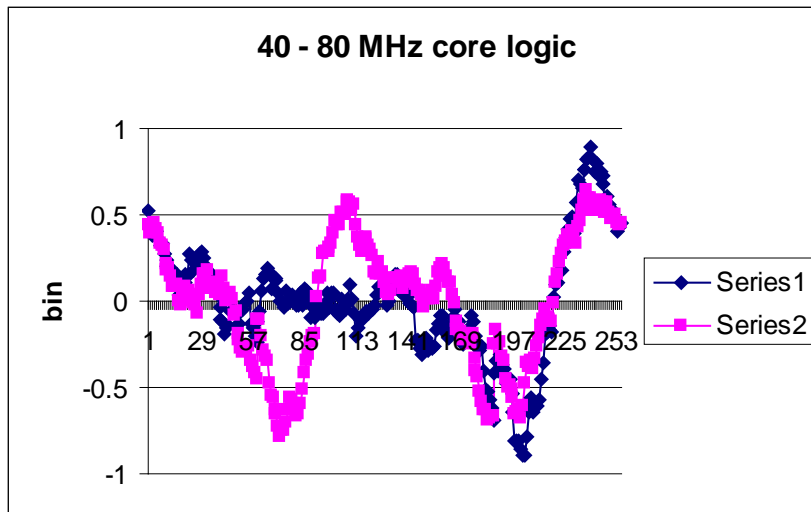
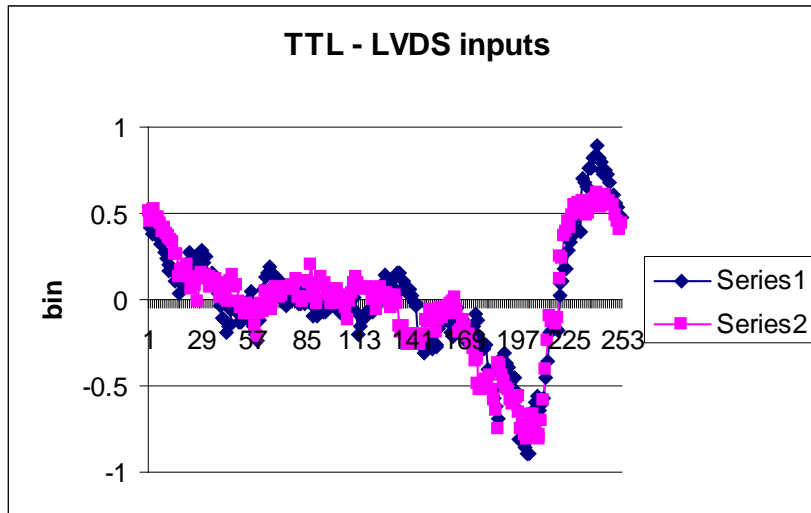
Measurements from ALICE-TOF

Effective RMS resolution:

- 40ps
- 17ps with table correction



HPTDC: Cause of INL Errors



It is clear that INL imperfections come from on-chip crosstalk from logic part of chip.

Several improvements have been made with limited improvement:
(special package with power/gnd plane, re-optimized signal routing, separation of power domains, etc.)

As logic clock is the same as the time reference for the time measurements this is a fixed pattern that can be compensated for if needed with a simple table look-up

HPTDC: SEU Handling

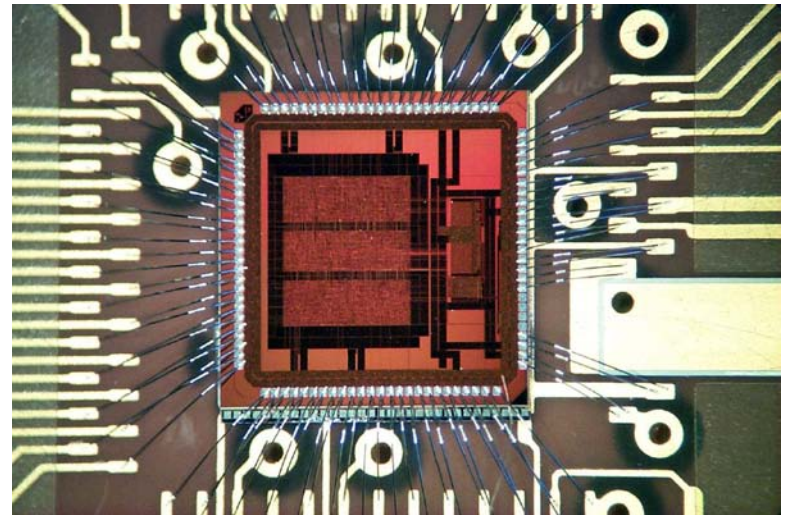
- ❑ SEU detection (not SEU immune)
- ❑ Programming data protected with parity check
- ❑ All internal memories have parity check
- ❑ State machines implemented with one hot encoding and continuous state check
- ❑ Measurements with parity error ignored in matching
- ❑ Error status with information about detected parity errors from different functional blocks
- ❑ Programmable global error state which can force the TDC into a passive state

Data Transmission in HEP

- Data acquisition and trigger systems in the LHC require
 - 40,000 "analogue Links"
 - > 25,000 Gbit/s digital links
- These links are unidirectional:
 - Transmitters inside the detectors
 - Receivers in the counting rooms
- Transmitters are subject to high levels of radiation doses over the lifetime of the experiments:
 - No commercial product available
 - CERN to developed their own radiation tolerant high speed serializer and analogue links

Gigabit Optical Link (GOL)

- Two encoding schemes:
 - G-link
 - Gigabit Ethernet (8B/10B)
- Transmission speed:
 - Fast: 1.6 Gbit/s , 32 bit data input @ 40 MHz
 - Slow: 0.8 Gbit/s , 16 bit data input @ 40 MHz
- Synchronous (constant latency)
- Drivers:
 - Laser driver
 - 50 Ω driver
- Interfaces for control and status:
 - I2C
 - JTAG



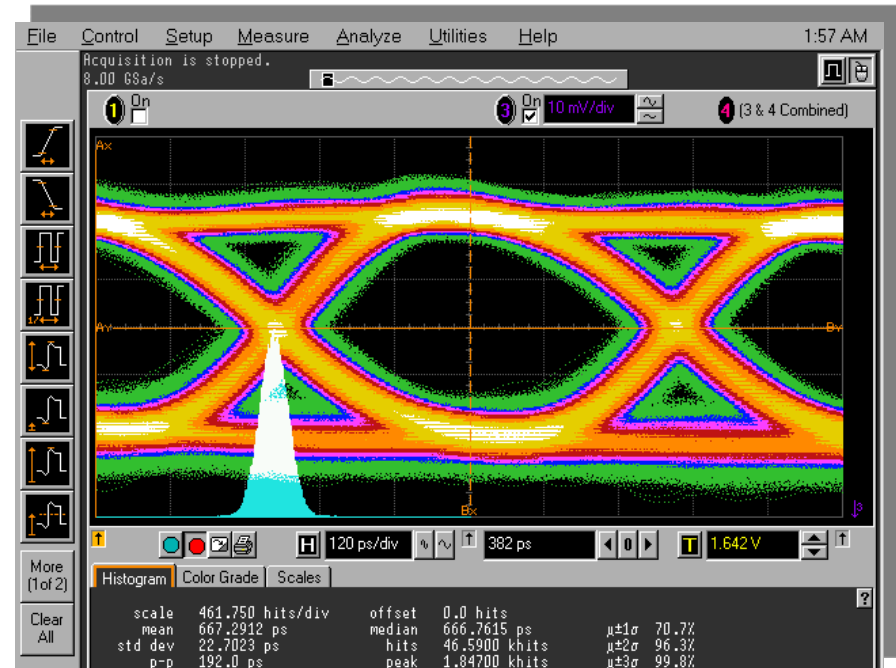
GOL: Improving the SEU Tolerance

- Digital logic: different approaches adopted throughout the IC:
 - Configuration data:
 - hard-wired logic values
 - Configuration settings:
 - Hamming code protected memory
 - Data path:
 - Triple modular redundancy with majority voting
 - State Machines:
 - Triple modular redundancy with majority voting

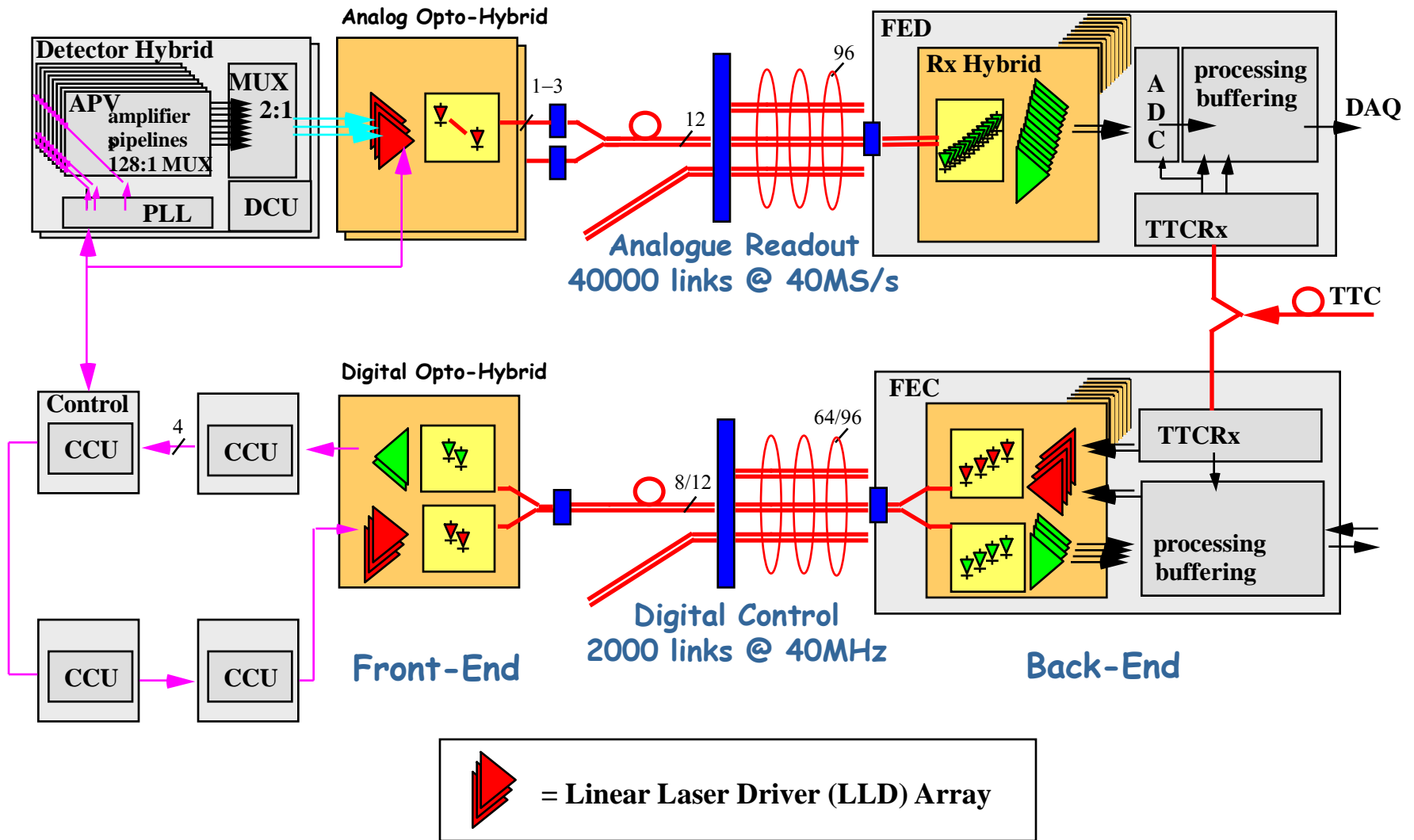
GOL: Improving the SEU Tolerance

- Fast logic:
 - Increased size transistors
- Analog circuits:
 - Bias currents doubled were possible.
 - Loop-filter “impedance” reduced, maintaining loop-dynamics.
 - Node capacitance increased for “standstill” nodes.
- All this at the price of added power consumption:
 - 800 Mbit/s \Rightarrow 275 mW (includes 7.8 mA VCSEL bias current)
 - 1.6 Gbit/s \Rightarrow 390 mW (includes 7.8 mA VCSEL bias current)

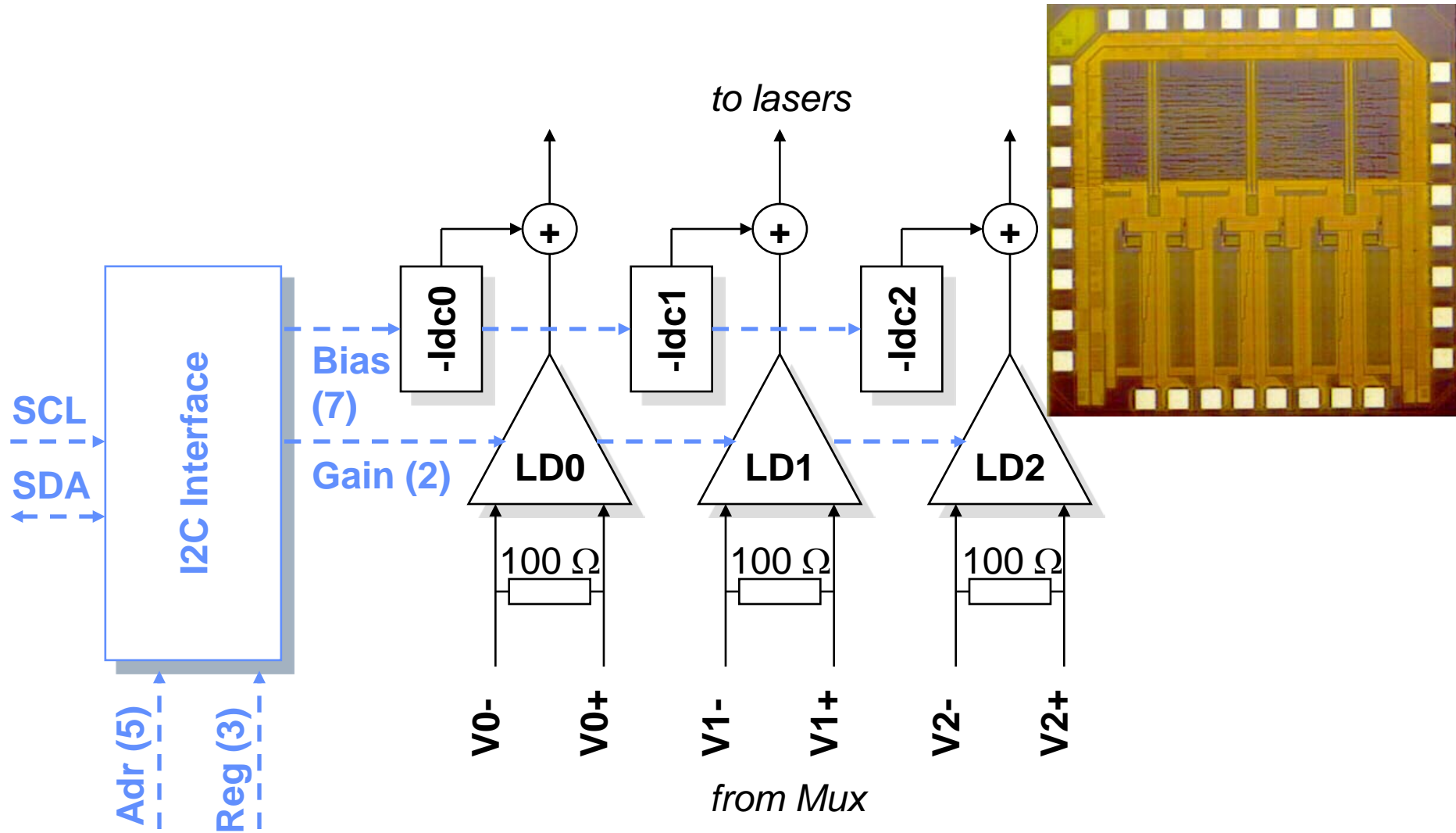
EELD: 1.6 Gbit/s



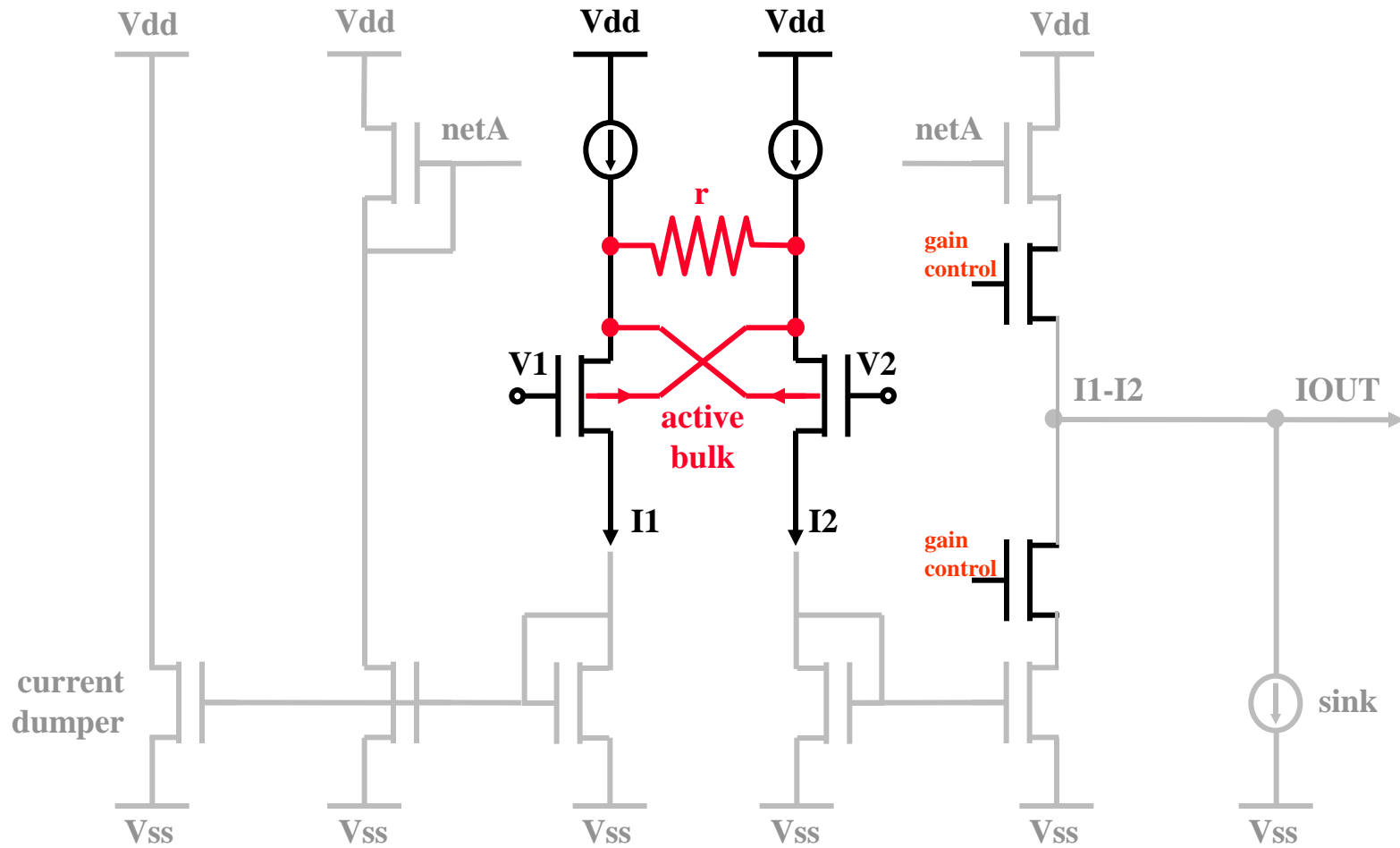
CMS Tracker Readout and Control Electronics



Linear Laser Driver (LLD)

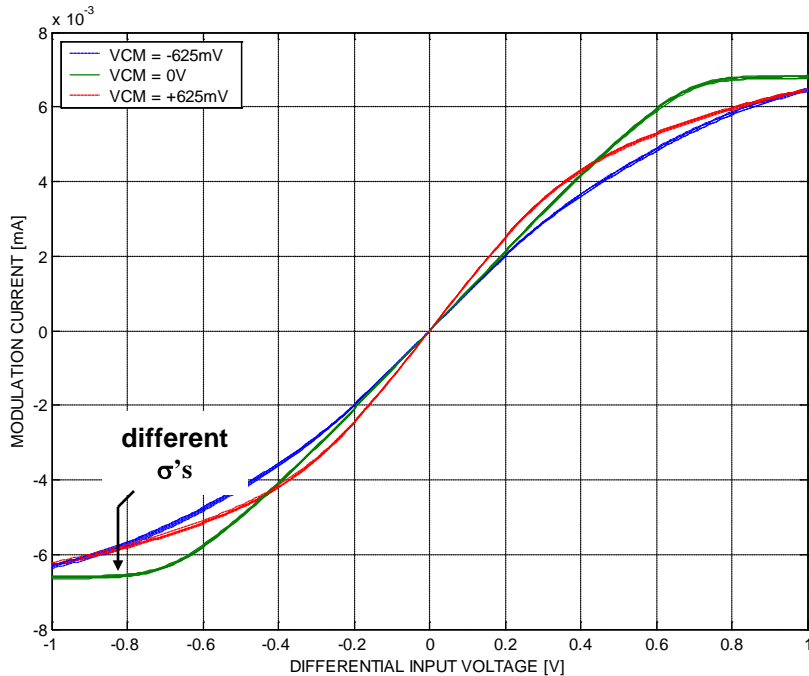


LDD: Circuit

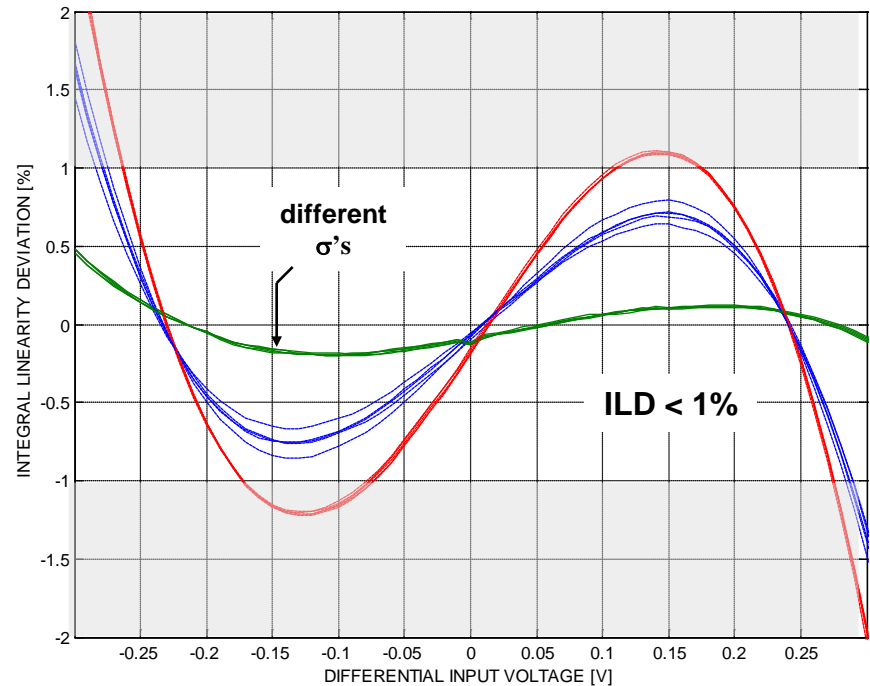


LLD: Gain and Linearity

TRANSFER CHARACTERISTIC



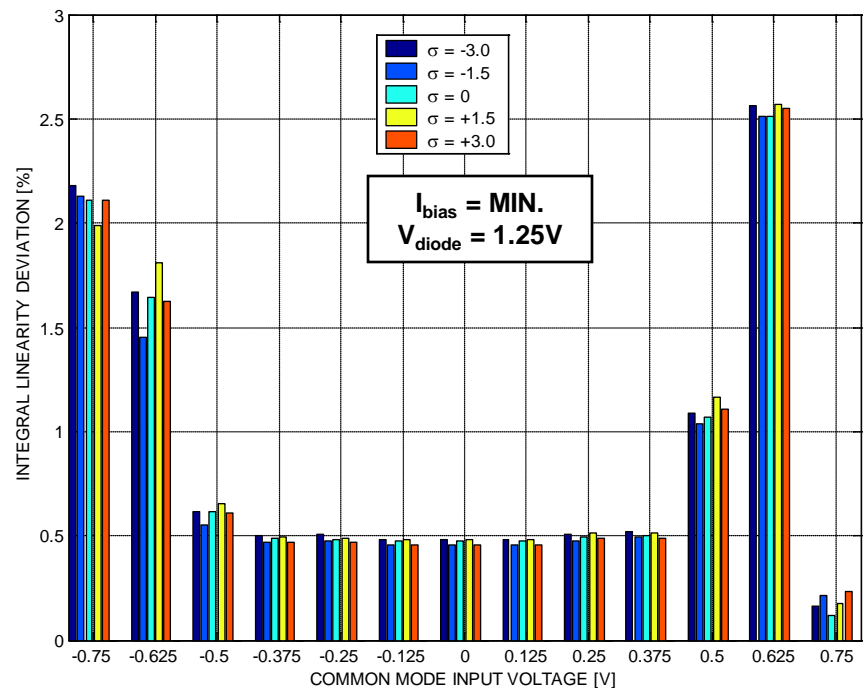
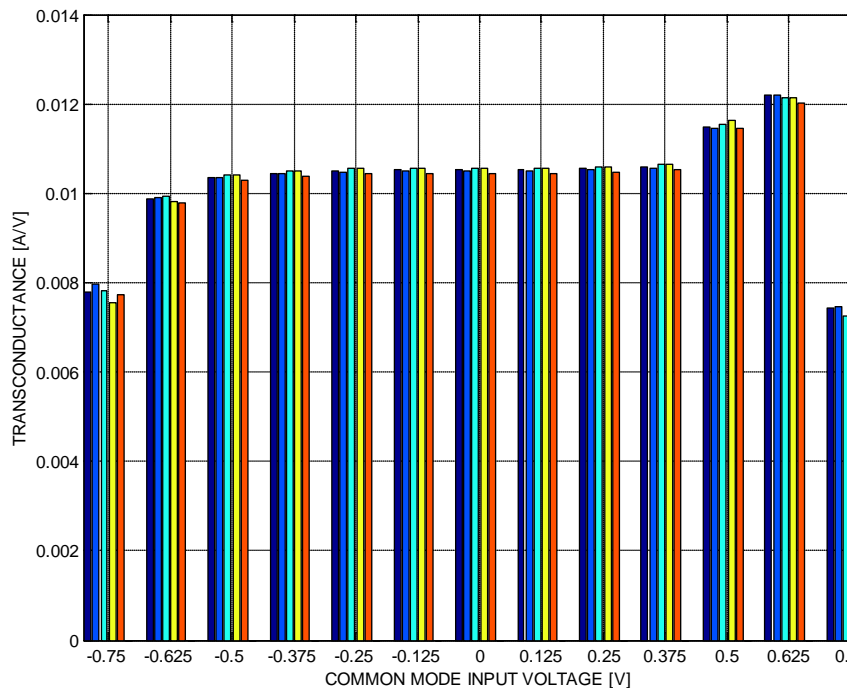
LINEARITY



- Linear operating range: $\pm 300\text{mV}$
- Integral linearity deviation: $< 0.5\%$ ($V_{cm}=0$)

Common Mode

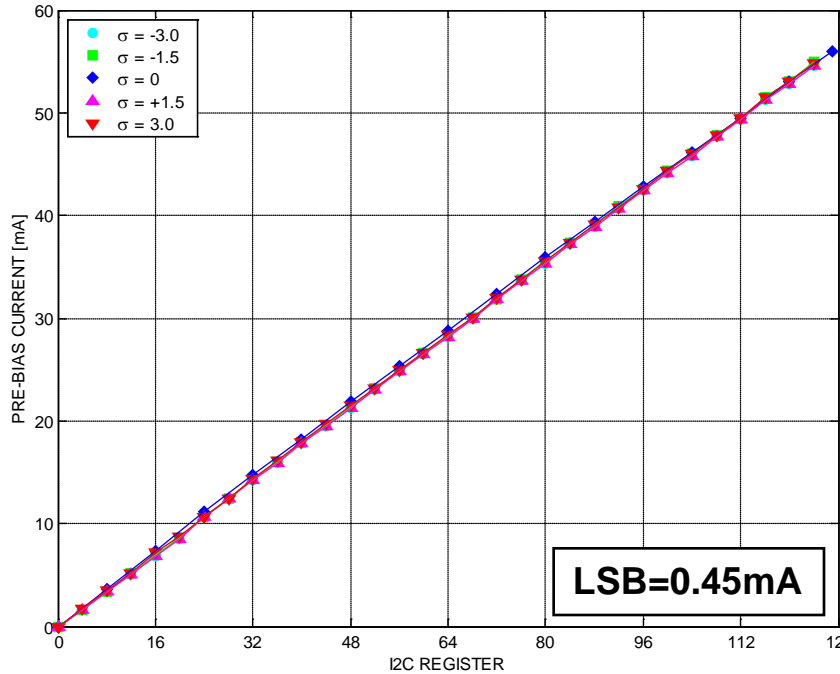
GAIN AND LINEARITY VS. INPUT COMMON MODE



- Input common-mode range: $\pm 350\text{mV}$ (for specified gain and linearity)

LLD: characteristics

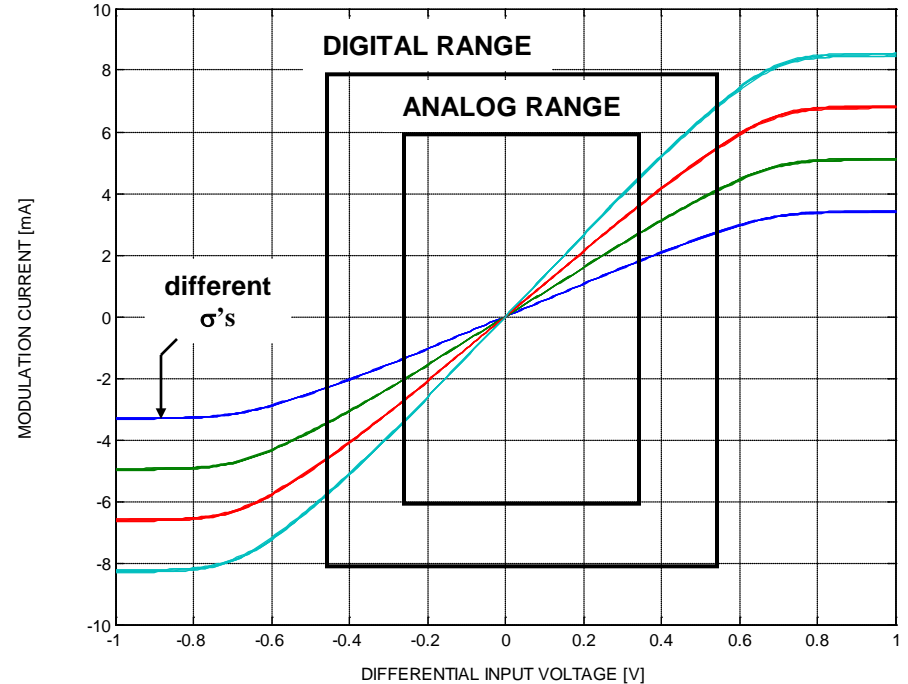
Laser Bias Current



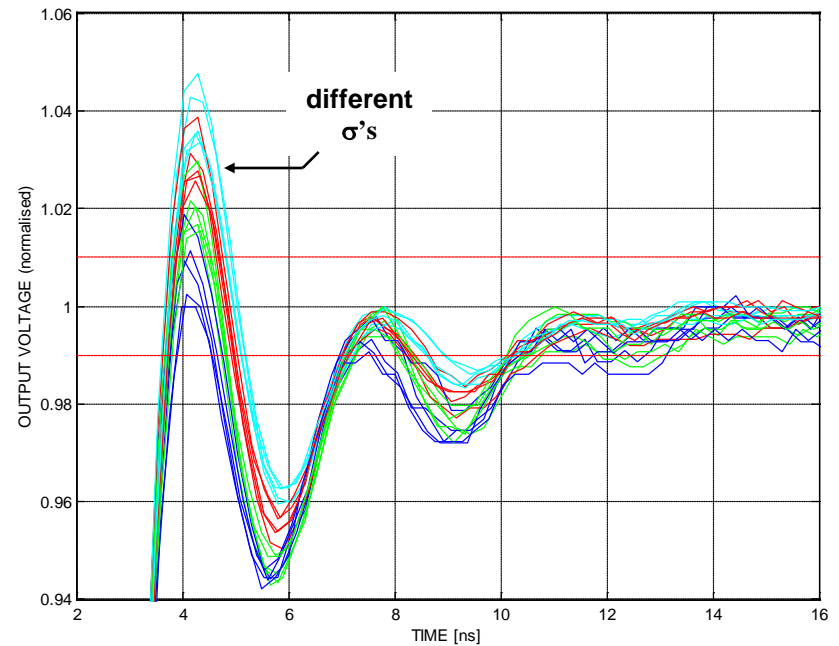
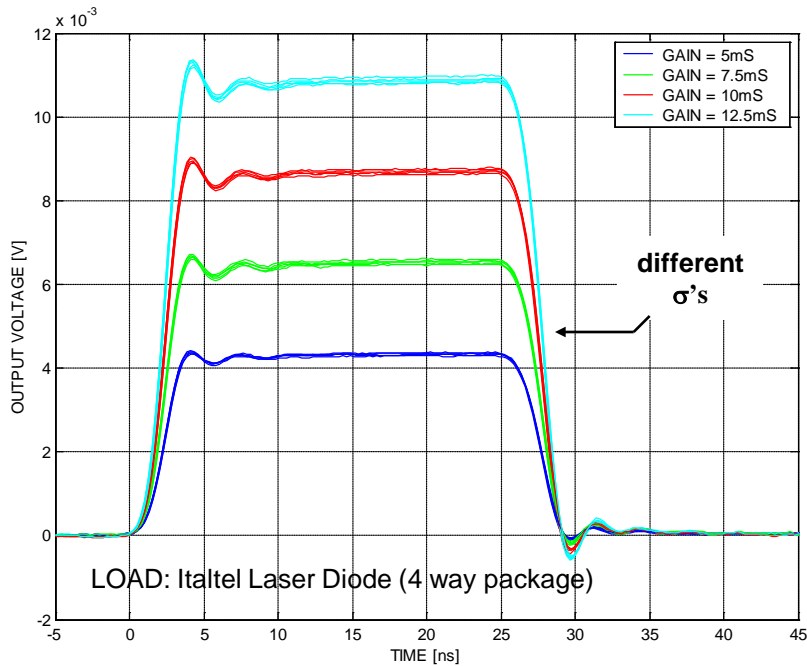
Programmable

- Laser bias: 55mA (7bits)
- Gains: 5mS, 7.5mS, 10mS, 12.5mS

Transfer Characteristics

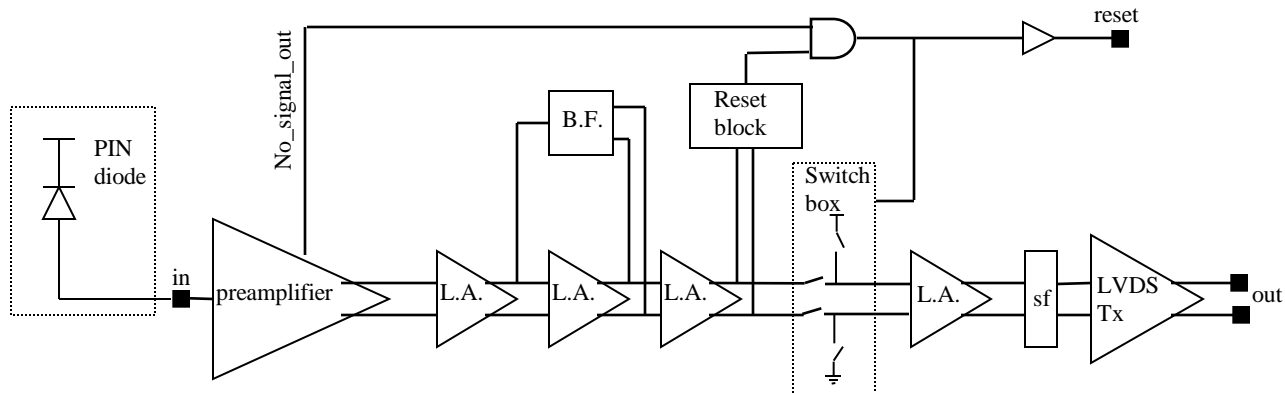


LLD: Time response

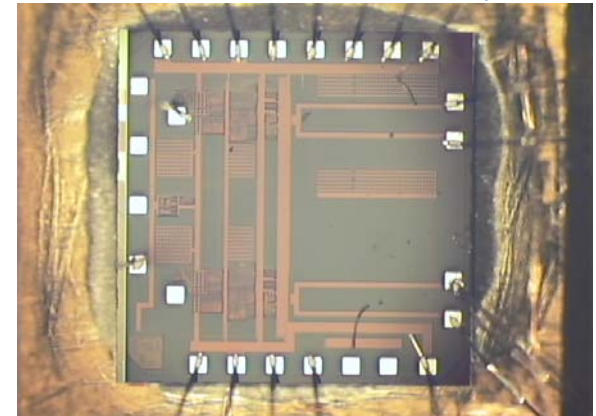


- Rise/Fall Times (10% to 90%): 2.5ns
- Settling Time (to 1% of final value): 10-12ns

RX40 Optical receiver

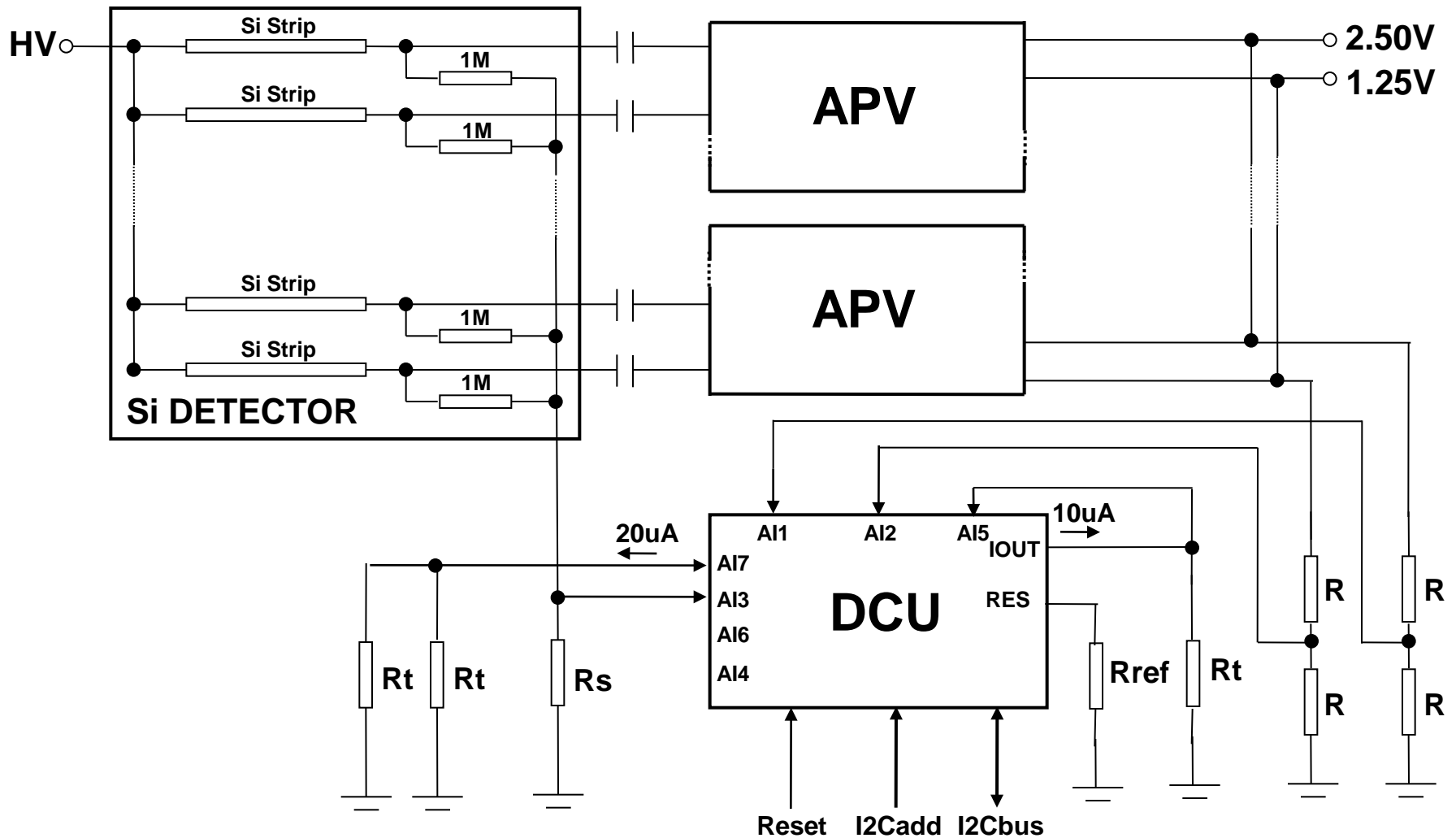


4 channels / chip

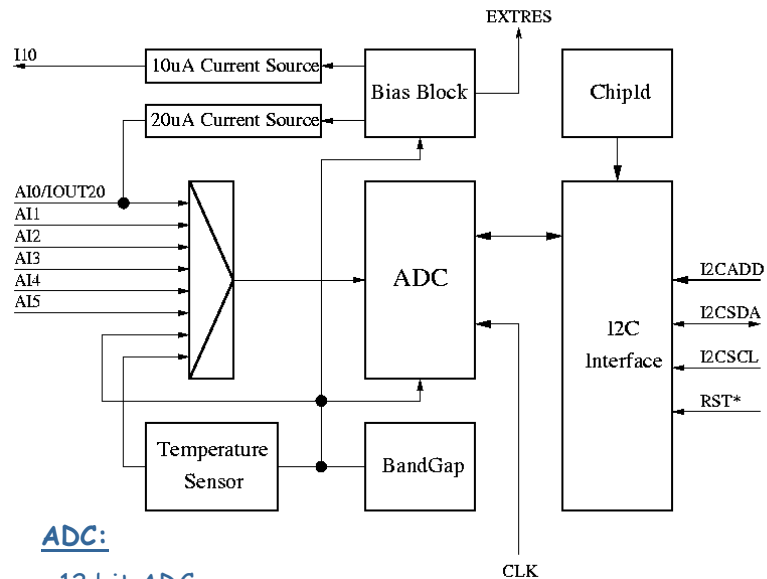


	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Note</i>
DC input current			500	μA	Baseline DC current
AC input current	10 (after rad)		500	μA	
Bandwidth	80			MHz	
Low cut-off frequency			1-2	MHz	
Jitter			0.5	ns	
Output voltage level		LVDS			
Supply voltage		2.5		V	
Sensitivity		-20		dBm	
Bit error rate		10^{-12}			
Reset output					Low for $>5\mu\text{s}$ for a transmission of 20 consecutive '0'
Coupling with p-i-n diode		DC			
Diode bias voltage		1.8		V	

Detector Monitoring System



DCU Architecture

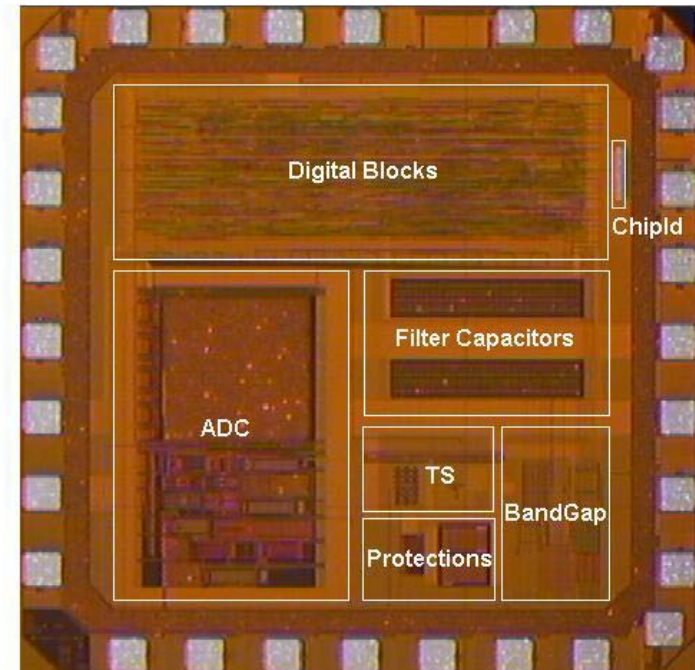


ADC:

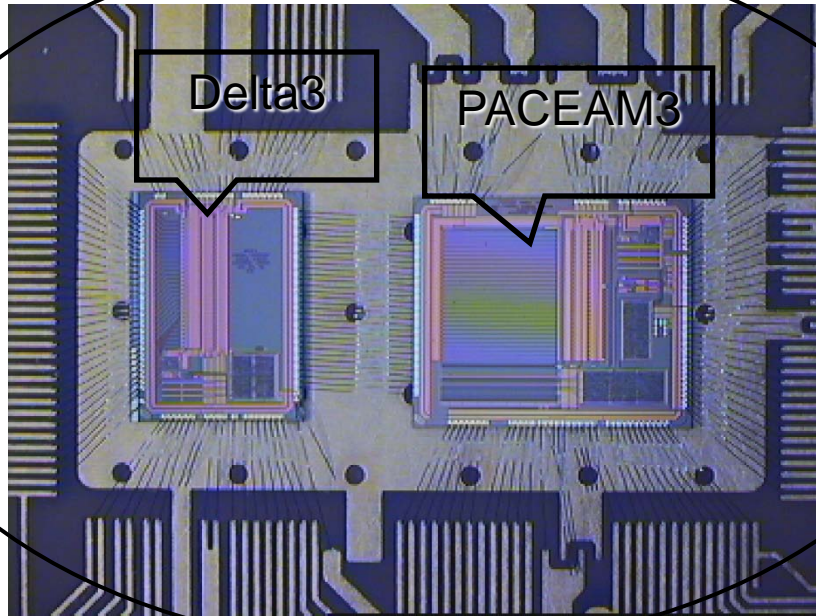
- 12 bit ADC
- $|INL| < 1 \text{ LSB}$ (in the input range)
- $|DNL| < 1 \text{ LSB}$ (monotonic characteristic, no missing codes)
- Noise RMS $< 0.5 \text{ LSB}$ (transition noise)
- Conversion time: 0.25 ms (maximum value)
- Power Consumption: $< 40 \text{ mW}$

Integrated Temperature sensor:

- Gain = 9.22 LSBs/C (resolution $\sim 0.108 \text{ C}$)
- Out @ 25C 2469 (RMS = 32.3) \Rightarrow Calibration required
- INL $< 2.5 \text{ LSBs}$ (-30C \rightarrow +30C)

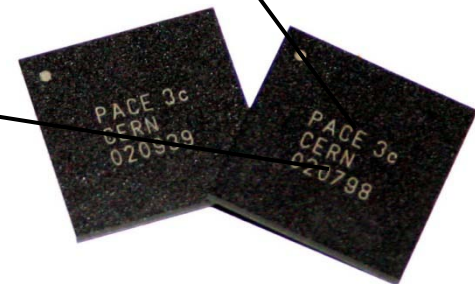


PACE3



Assembly of two ASICs
Delta3 and PACEAM3

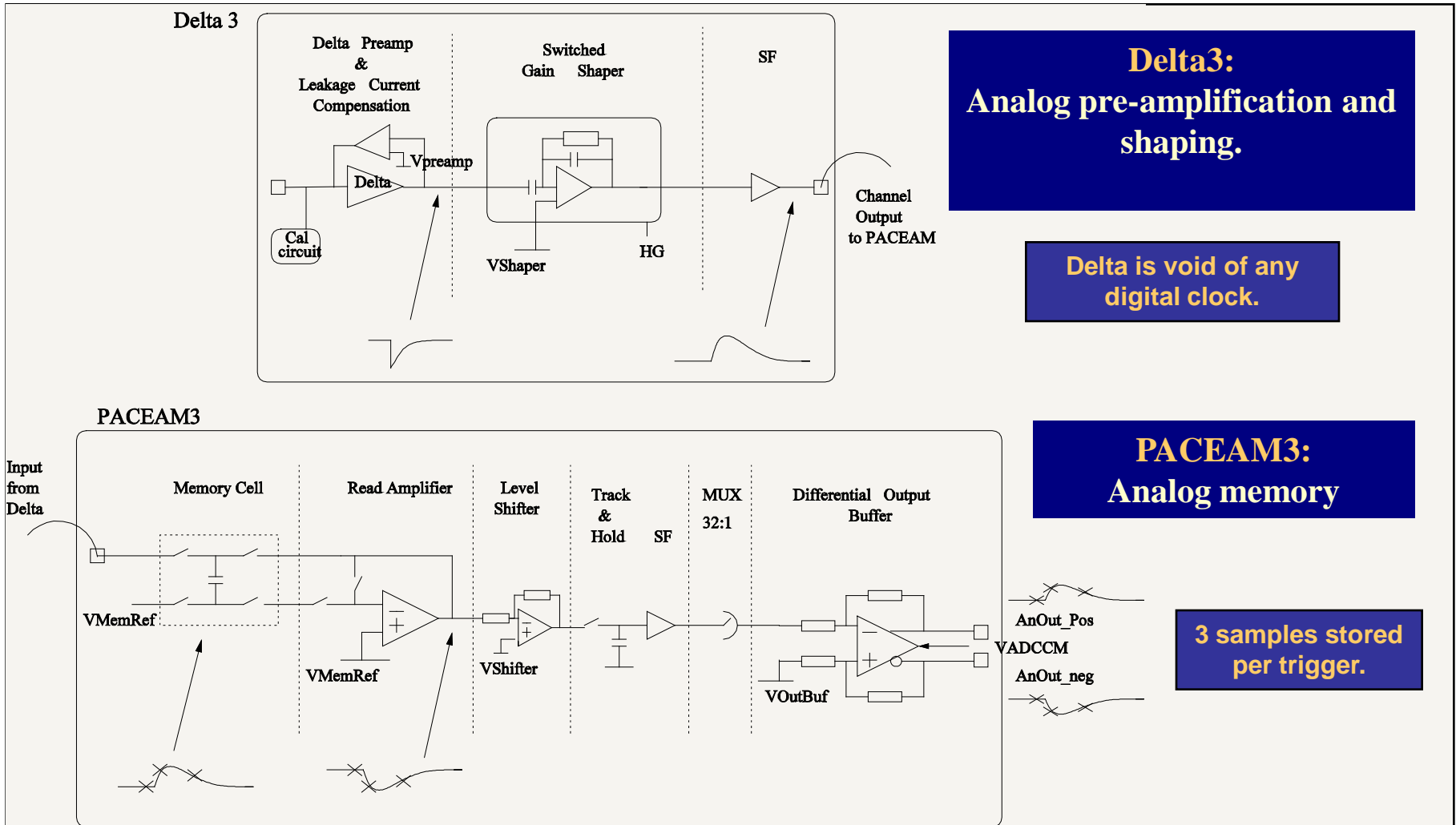
Packaged within a
196 pin FPBGA



ASIC Technology
0.25 μ m CMOS

2.5V power supply

PACE3 analog chain



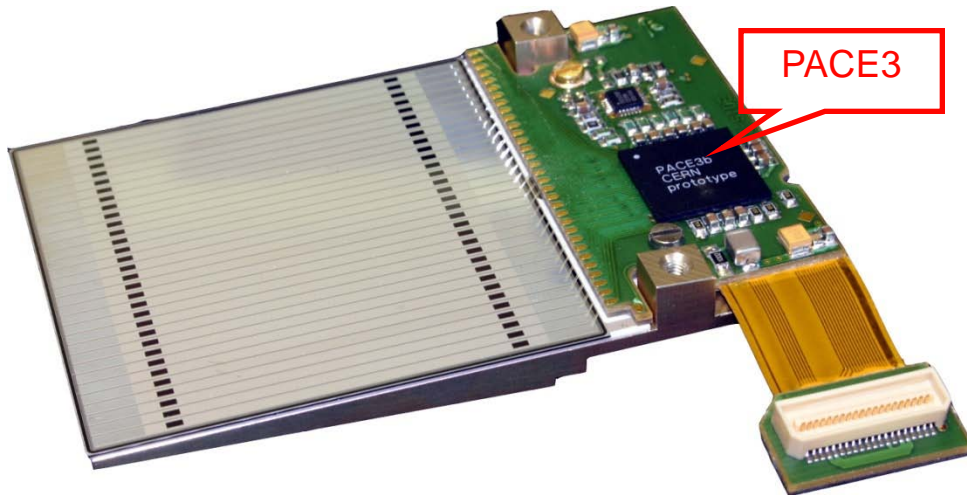
Delta3:
Analog pre-amplification and shaping.

Delta is void of any digital clock.

PACEAM3:
Analog memory

3 samples stored per trigger.

PACE3 with Preshower Si Sensors



The Preshower Micro-module

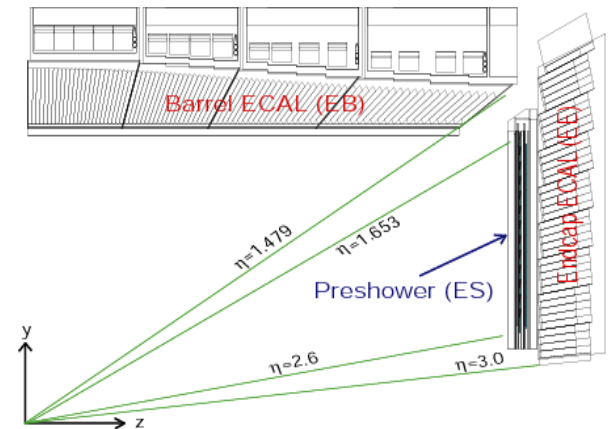
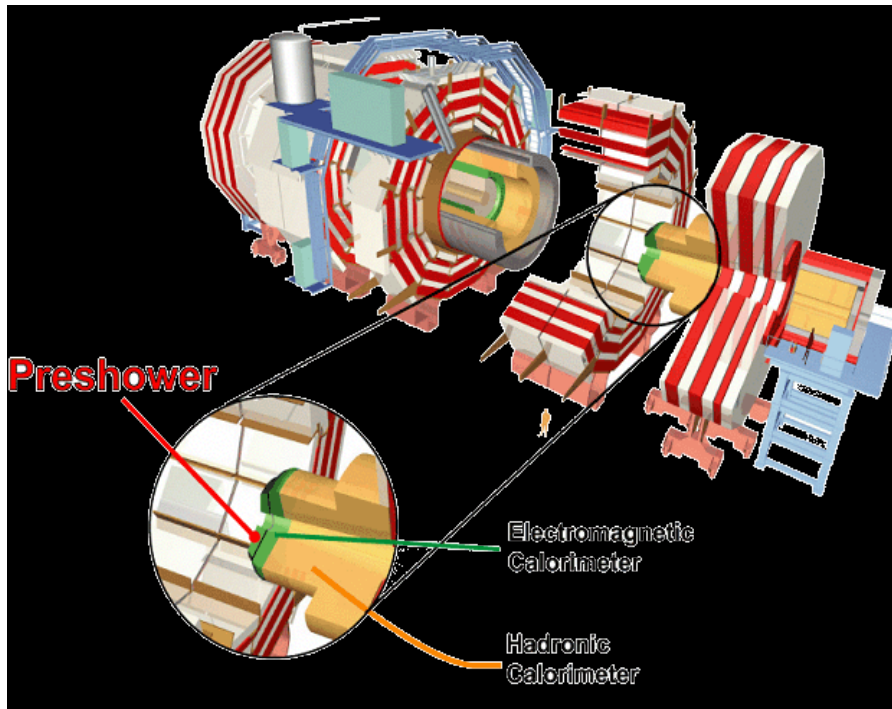
Silicon sensor ($\sim 61\text{mm} \times 61\text{mm}$)
32 channels
(1.875 mm channel pitch)

Silicon thickness = $320\mu\text{m}$
1 Minimum Ionising Particle deposits an average of 3.7 fC of charge (23257 e)

PACE3 Design Application

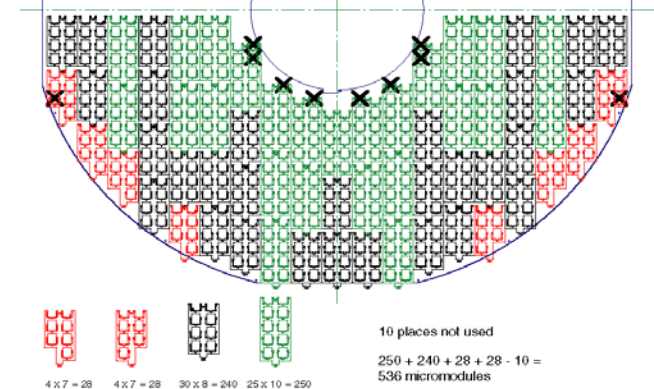
The CMS Preshower Detector for LHC

~ 4300 sensors
4.1 m² active silicon per disc



2 layer sampling calorimeter to detect photons with a good spatial resolution for τ/τ rejection. Incident photons on lead absorbers initiate electromagnetic showers of electrons, positrons and photons.

Preshower Disc



VFAT2 Functions

- **Trigger**
 - Provide intelligent “FAST OR” information as an input for the first level trigger (LV1A).
 - Programmable segmentation for Roman Pot and GEM configurations.

- **Tracking**
 - Binary “hit” information for each of the 128 channels as triggered by the LV1A.

Reference for VFAT2:

“VFAT2: A front-end system on chip providing fast trigger information, digitized data storage and formatting for the charge sensitive readout of multi-channel silicon and gas particle detectors.”

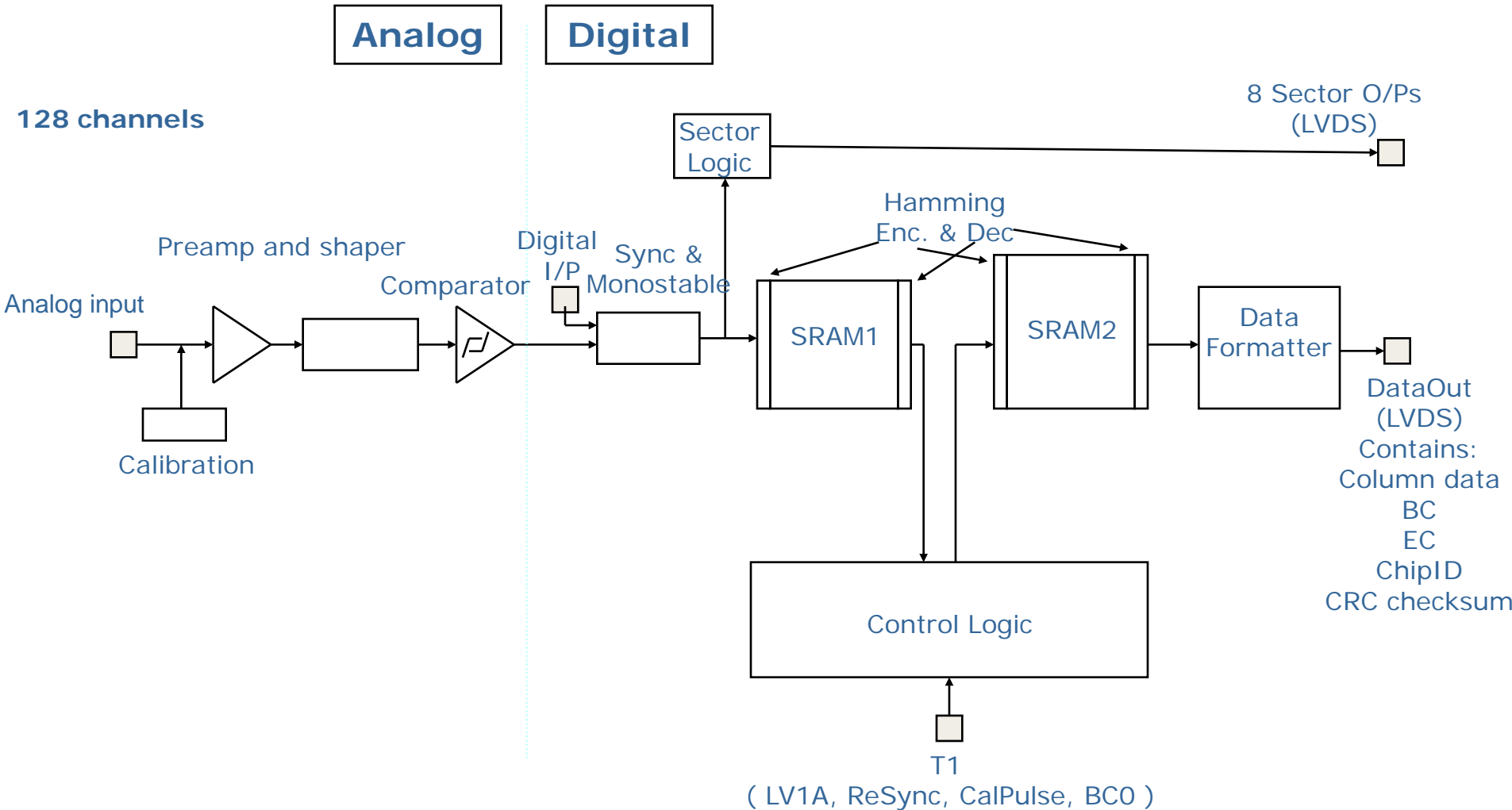
Proceedings of TWEPP Prague, Czech Republic, 3-7 September 2007, ISBN 978-92-9083-304-8, p.292 .

VFAT2 Key Features

Trigger and Tracking Functions

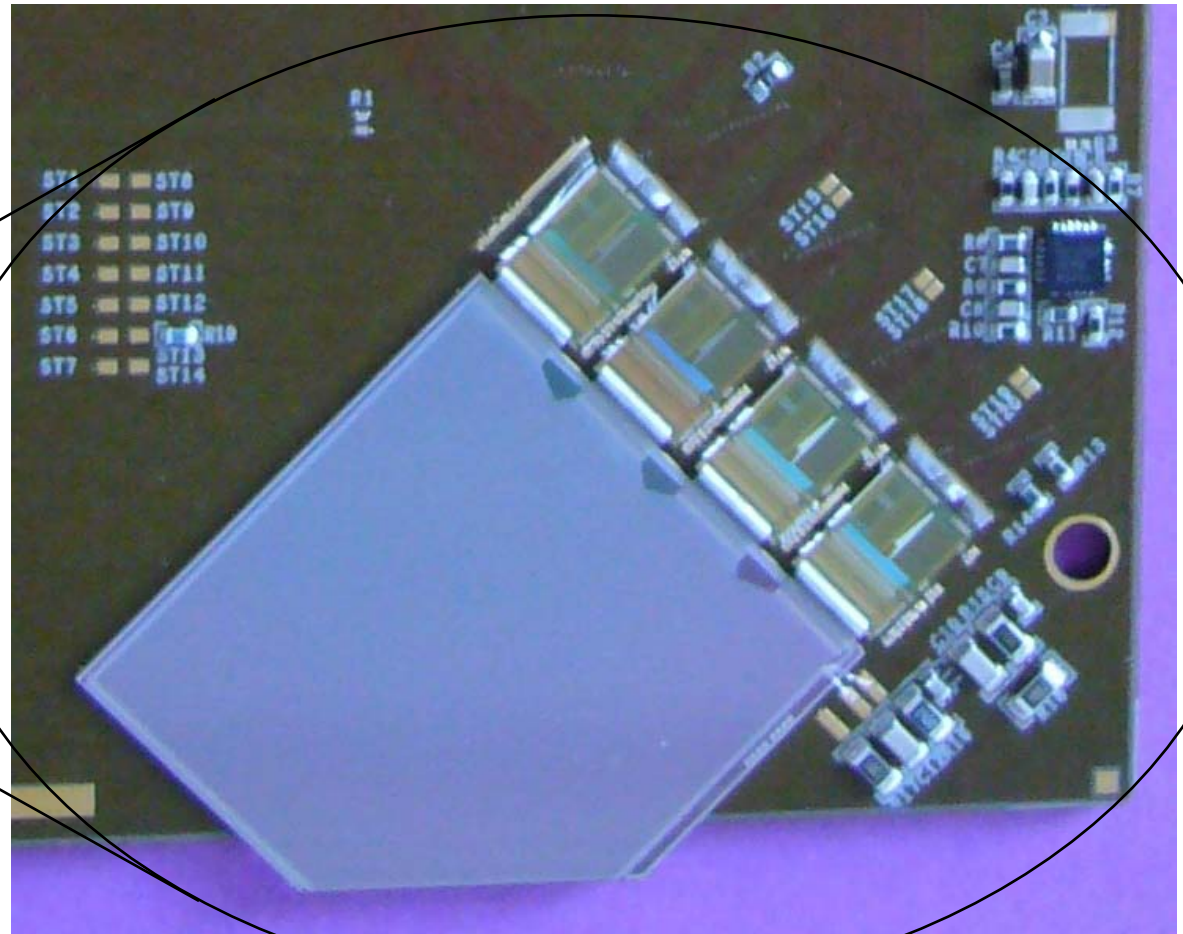
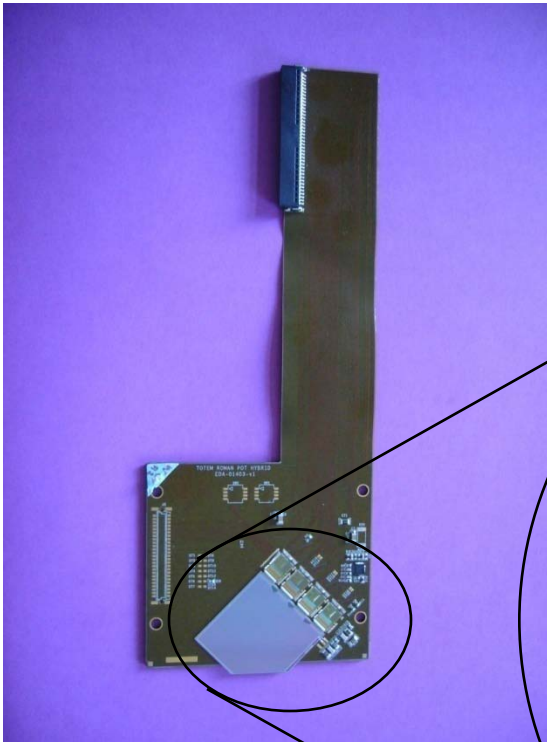
- **128 channel**
 - low noise front-end chip for binary readout of capacitive sensors.
- **40MHz signal sampling**
 - dead time free
- **Digital memory**
 - Programmable LV1A latency up to 256 clock periods.
 - Simultaneously storage of up to 128 triggered events.
- **Trigger building**
 - Programmable “fast-OR” trigger building outputs
- **Internal calibration**
 - via internal test pulses with programmable amplitude
- **Fully programmable**
 - through an I2C interface.
- **Data packet output**
 - includes headers, counters, flags and CRC check
- **Radiation tolerant design**
 - suitable for use in demanding radiation environments both with respect to ionizing radiation and Single Event Upset.

VFAT2 Signal Flow



Totem Si Sensor with 4 VFATs

Totem Roman Pot board with 4 VFATs

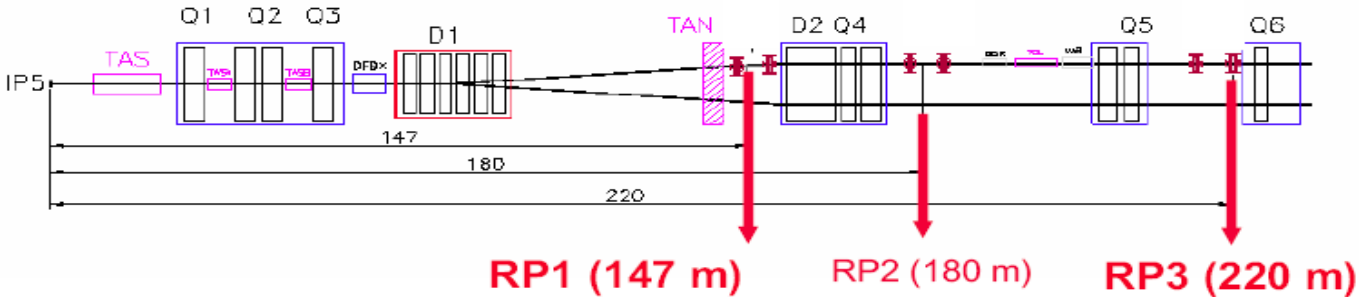
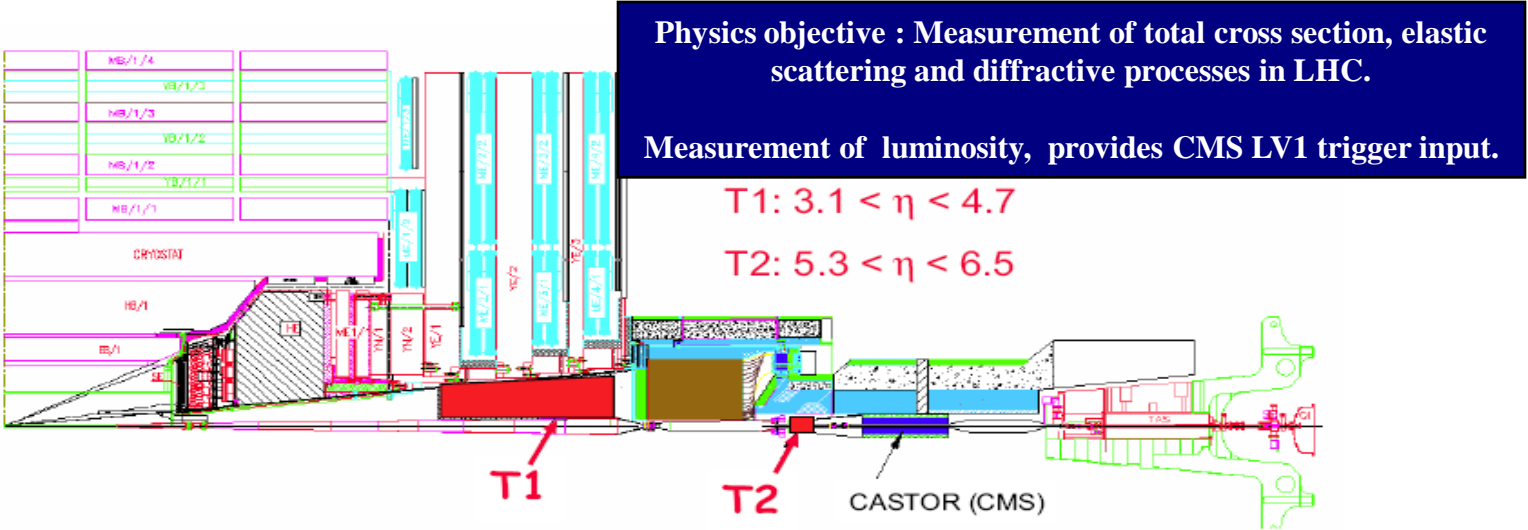


Silicon strips
512 channels
4 VFATs
Noise $\sim 1000 e / \text{channel}$

VFAT2 Design Application

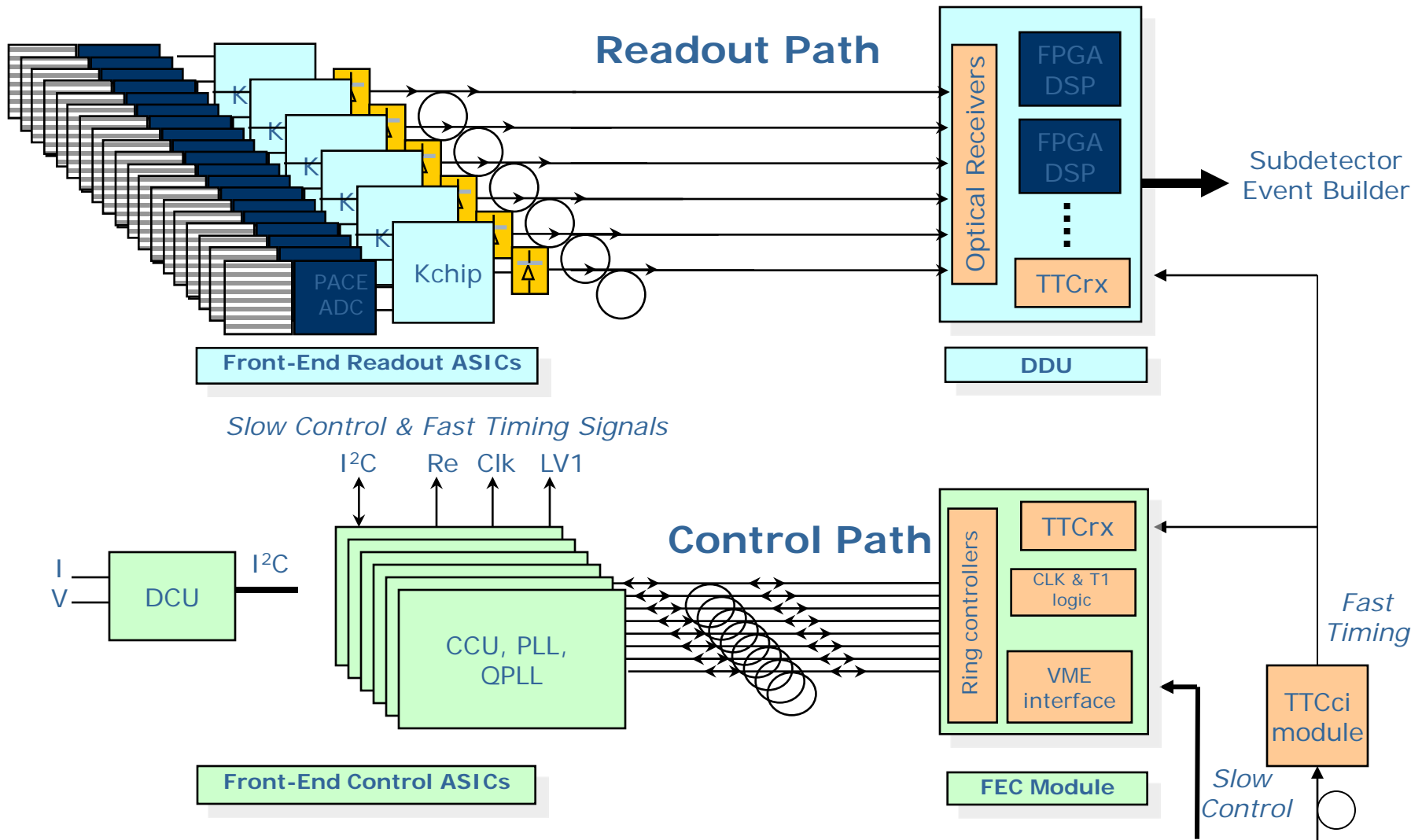


TOTEM in LHC

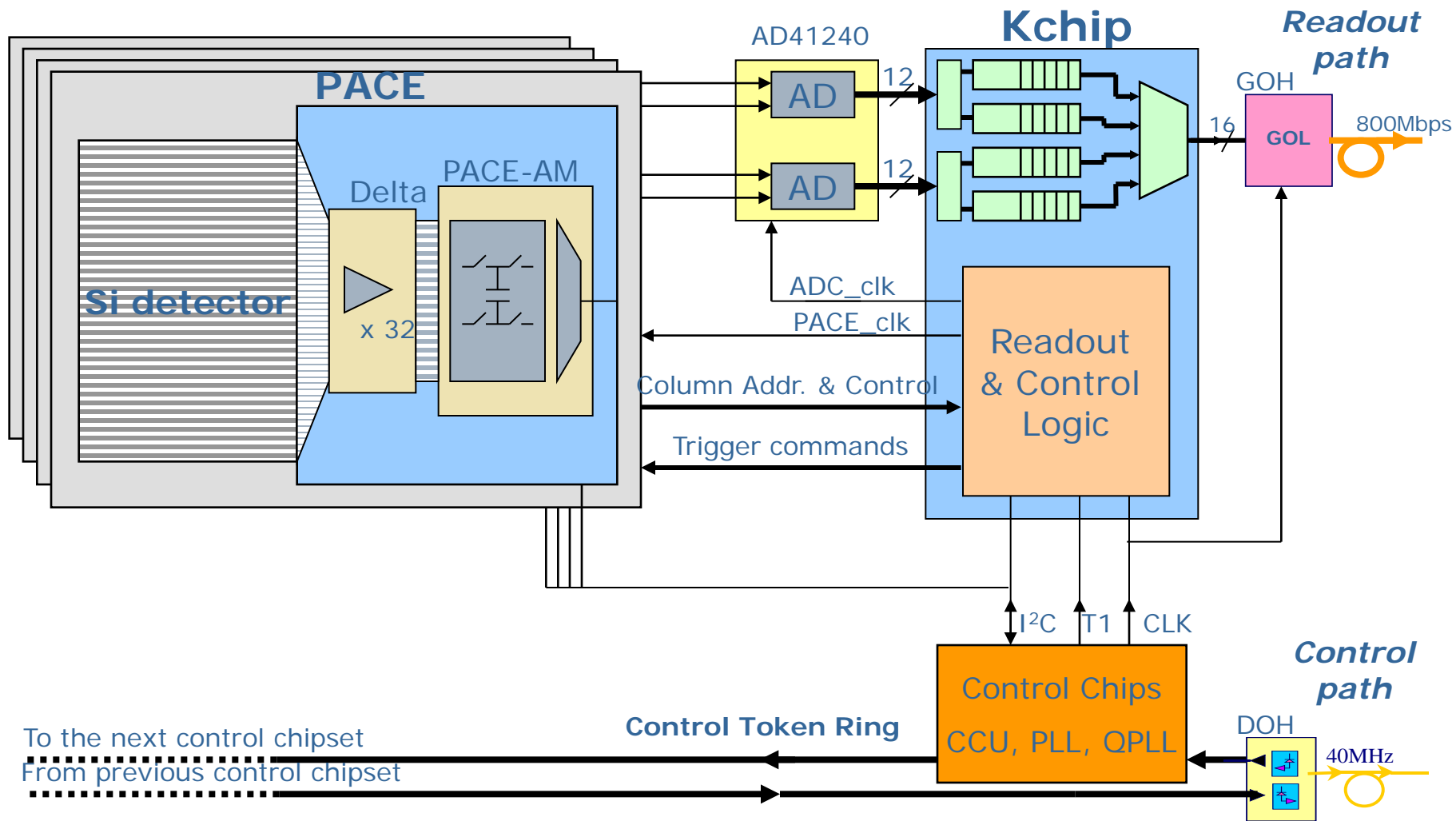


K.Eggert/CERN

Preshower Front-End System



Preshower Front-End Readout



Kchip Functionality

□ Data Concentration

- Can be configured to readout 1~4 PACE chips.

□ Event Data Formatting

- Align data into 16-bit words.
- Assemble an Event Packet.
- Assign a Bunch Count (BC) and Event Count (EC) Identifier.
- Link Protocol for transmission through a Gigabit Optical Link.

□ Readout Controller

- Trigger Command Decoding
- PACE Readout Synchronization Monitoring
- Front-End Buffers Overflow Detection / Prevention
- PACE & ADC clock and Trigger Command Distribution

Kchip Layout

1st Prototype

CERN MPW10

Submitted: Feb. 2003

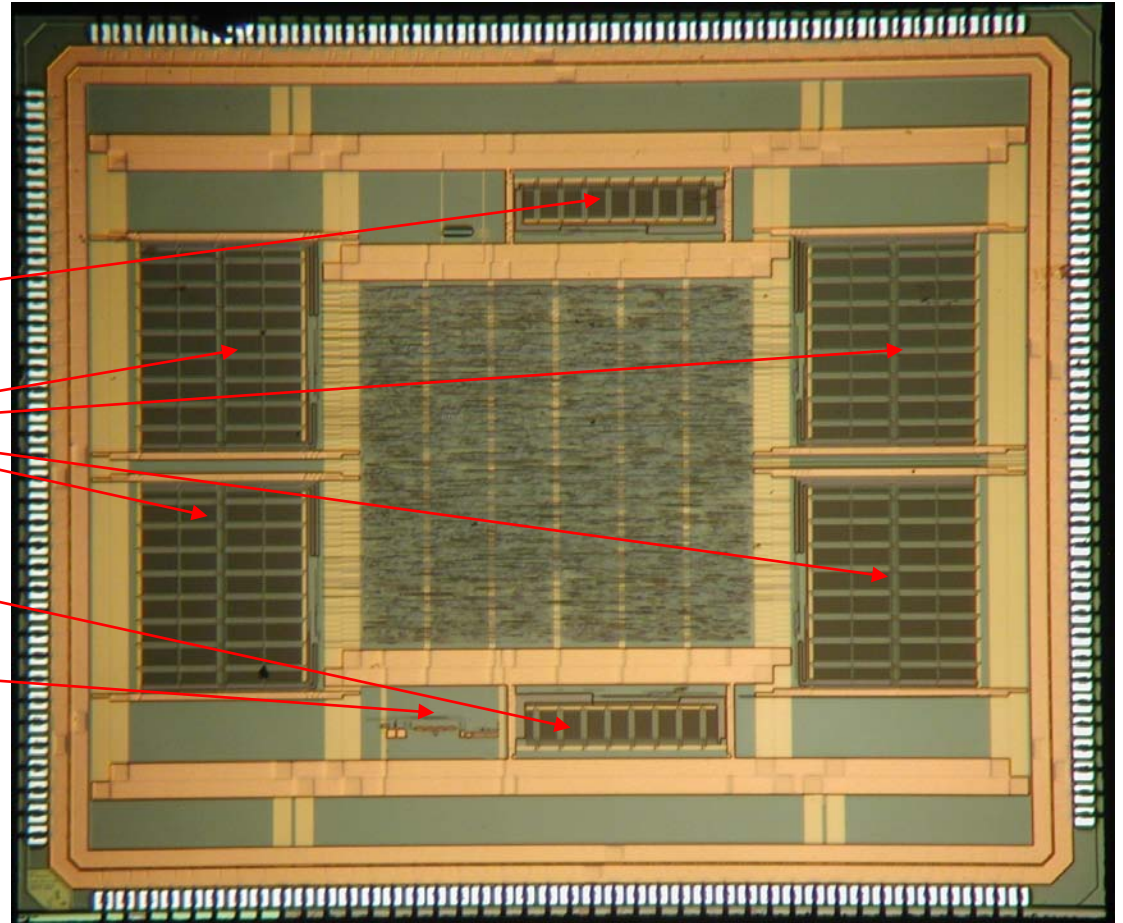
Received: June 2003

Column Addr. FIFO

Data FIFOs

Trigger FIFO

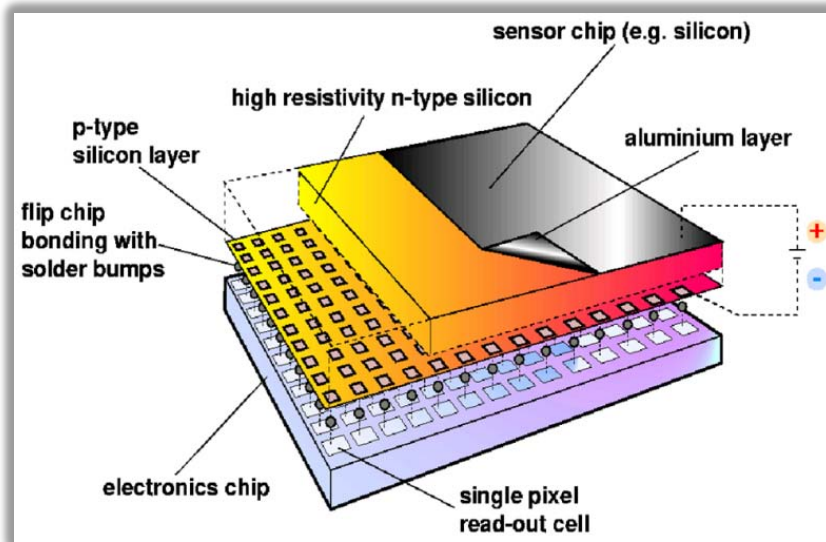
DLL block



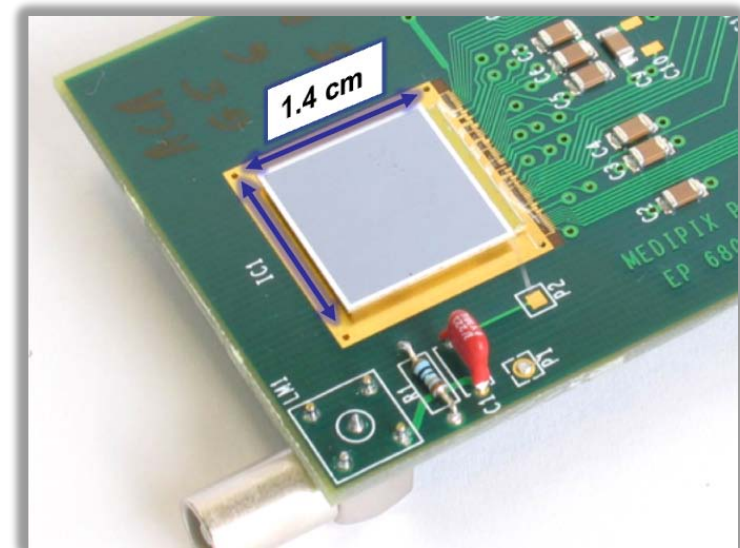
The Medipix Project

- International collaboration formed by 18 members to exploit the acquired knowledge at CERN in the design of particle track detectors in HEP to provide a noise-free X-ray imaging system with small spatial resolution ($55 \mu\text{m}$).
- The Medipix chip uses direct detection single photon counting hybrid pixel detector approach:
 - Linear and unlimited dynamic range
 - Continuous data taking possible:
 - noise suppression, large SNR
 - Multi-thresholds \rightarrow energy discrimination

Schematic of an hybrid pixel detector



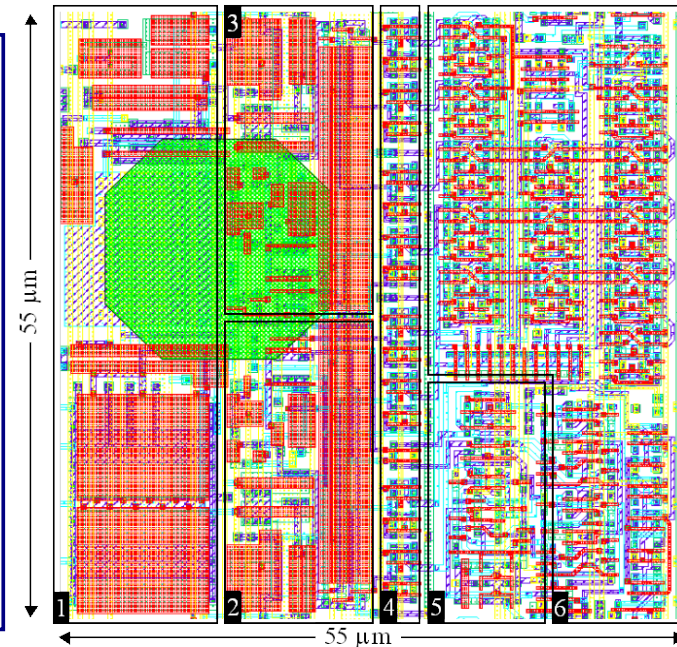
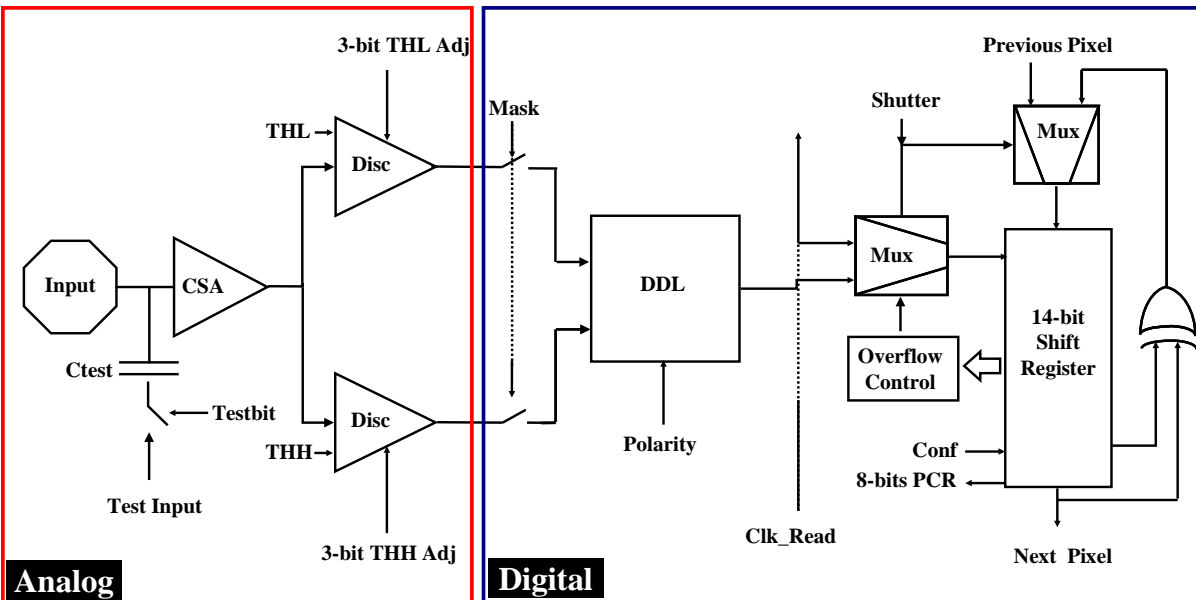
Medipix2 hybrid ($1.4 \times 1.4 \text{ cm}^2$)



Medipix2 pixel

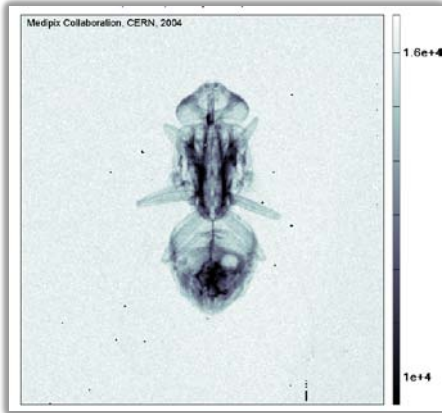
- The Medipix2 chip contains 256 x 256 pixels
- Pixel properties:
 - DC leakage current compensation per pixel
 - Sensitive to positive and negative input charges
 - Energy window discrimination (2 thresholds)
 - 3-bit threshold adjustment per threshold
 - 14-bit counter (11810 counts) per channel
 - Static power consumption is $8\mu\text{W}$ per pixel

Medipix2 schematic

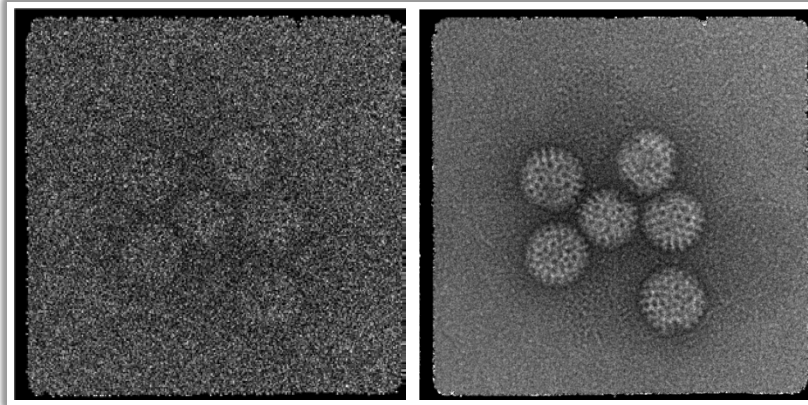


Applications using Medipix2

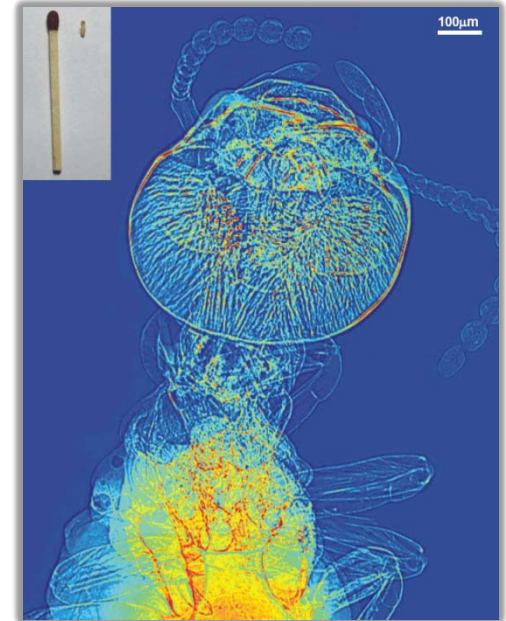
- Applications: Adaptive optics, X-ray diffraction, Micro-radiography, Neutron imaging, Computed tomography, Autoradiography, Gamma imaging, Electron microscopy, energy weighting, In vivo optical and radionuclide imaging, Micro-patterned gas detectors, Mammography...



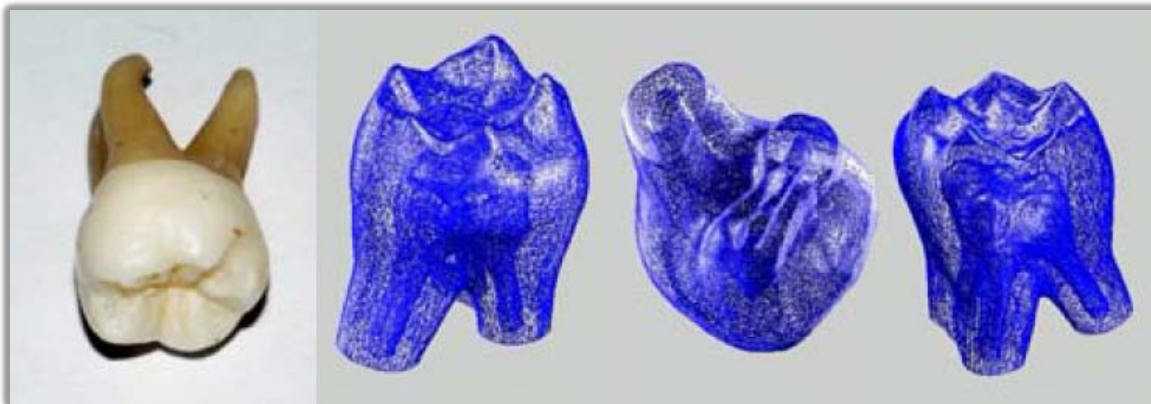
X-ray image of a house fly (CERN)



Electron microscopy: Rotavirus with 1.6 (left) and 160 (right) e^-/pixel , equivalent to: $0.04 e^-/\text{\AA}^2$ at specimen (left) and $4 e^-/\text{\AA}^2$ (right) (MRC, Cambridge)



Micro-radiography: Assembled radiograph of a termite. Real size of the image is approximately 1.4 mm x 1.7 mm (IEAP, Prague)



Neutron imaging: Photograph and tomographic 3D reconstructions of a tooth (IEAP, Prague)

<http://www.cern.ch/MEDIPIX>