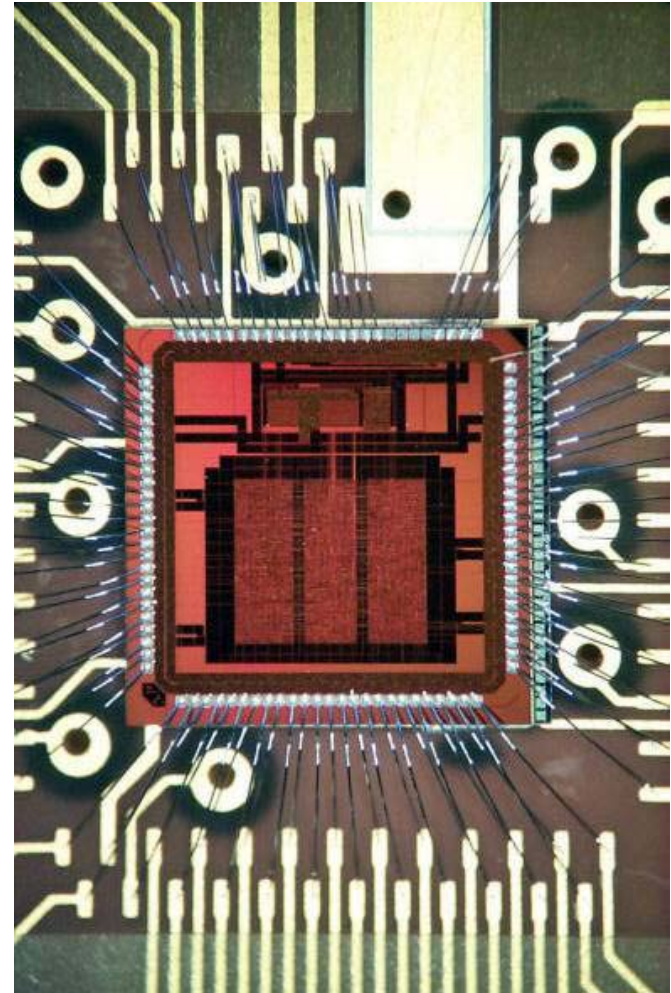


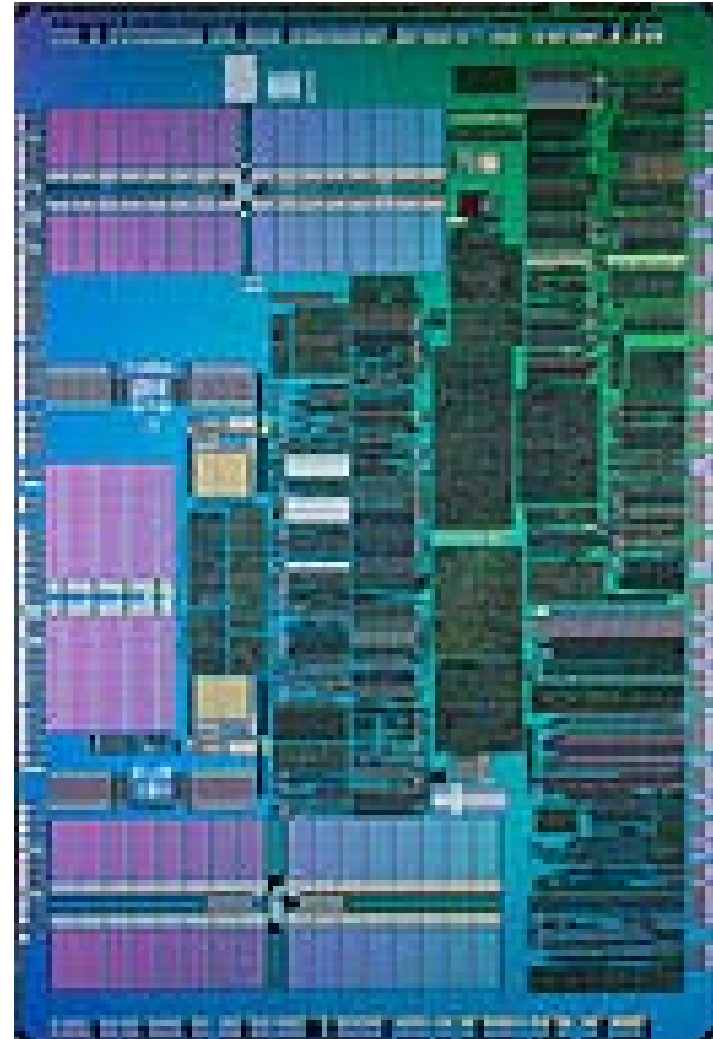
# Outline

- Introduction
- Transistors
- The CMOS inverter
- Technology
  - Lithography
  - Physical structure
  - CMOS fabrication sequence
  - Advanced CMOS process
  - Process enhancements
- Scaling
- Gates
- Sequential circuits
- Storage elements
- Phase-Locked Loops
- Example



# CMOS technology

- An *Integrated Circuit* is an electronic network fabricated in a single piece of a semiconductor material
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns
- The fabrication steps are sequenced to form three dimensional regions that act as transistors and interconnects that form the switching or amplification network



# Lithography

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Lithography: process used to transfer patterns to each layer of the IC

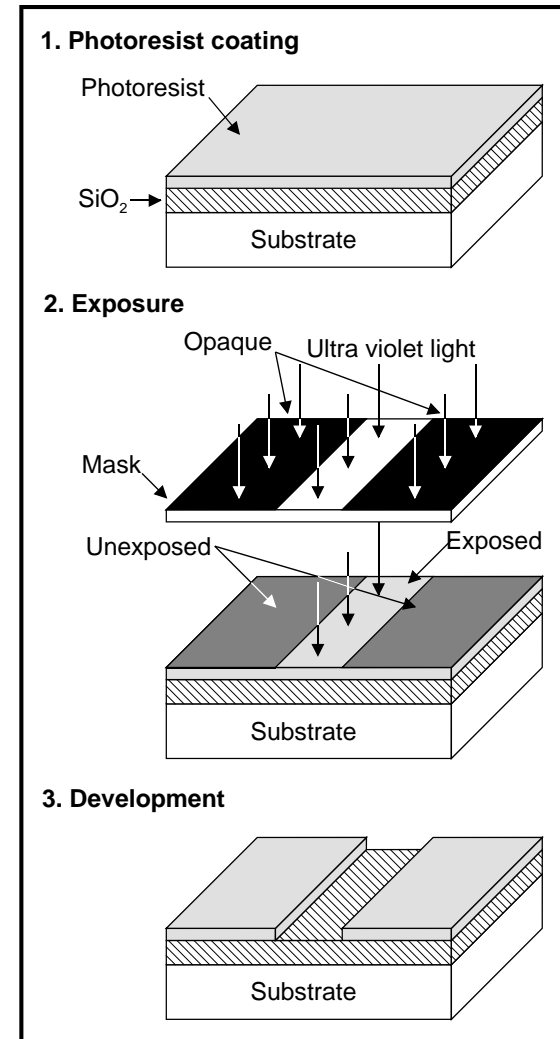
Lithography sequence steps:

- Designer:
  - Drawing the "layer" patterns on a layout editor
- Silicon Foundry:
  - Masks generation from the layer patterns in the design data base
  - Printing: transfer the mask pattern to the wafer surface
  - Process the wafer to physically pattern each layer of the IC

# Lithography

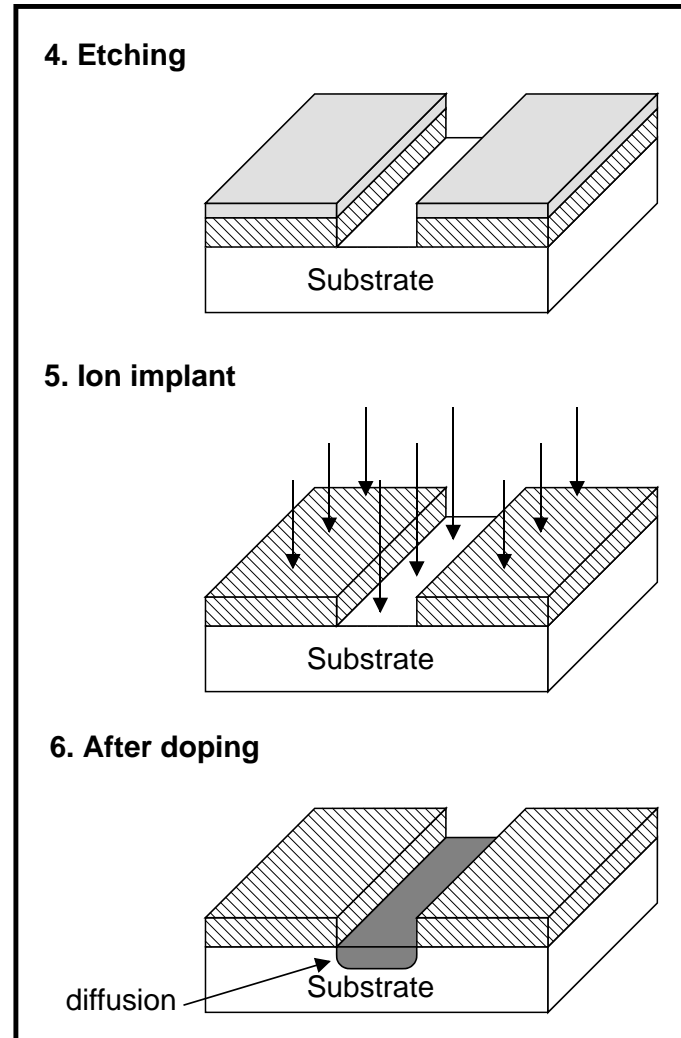
## Basic sequence

- The surface to be patterned is:
  - spin-coated with photoresist
  - the photoresist is dehydrated in an oven (photo resist: light-sensitive organic polymer)
- The photoresist is exposed to ultra violet light:
  - For a positive photoresist exposed areas become soluble and non exposed areas remain hard
- The soluble photoresist is chemically removed (development).
  - The patterned photoresist will now serve as an etching mask for the  $\text{SiO}_2$



# Lithography

- The  $\text{SiO}_2$  is etched away leaving the substrate exposed:
  - the patterned resist is used as the etching mask
- Ion Implantation:
  - the substrate is subjected to highly energized donor or acceptor atoms
  - The atoms impinge on the surface and travel below it
  - The patterned silicon  $\text{SiO}_2$  serves as an implantation mask
- The doping is further driven into the bulk by a thermal cycle



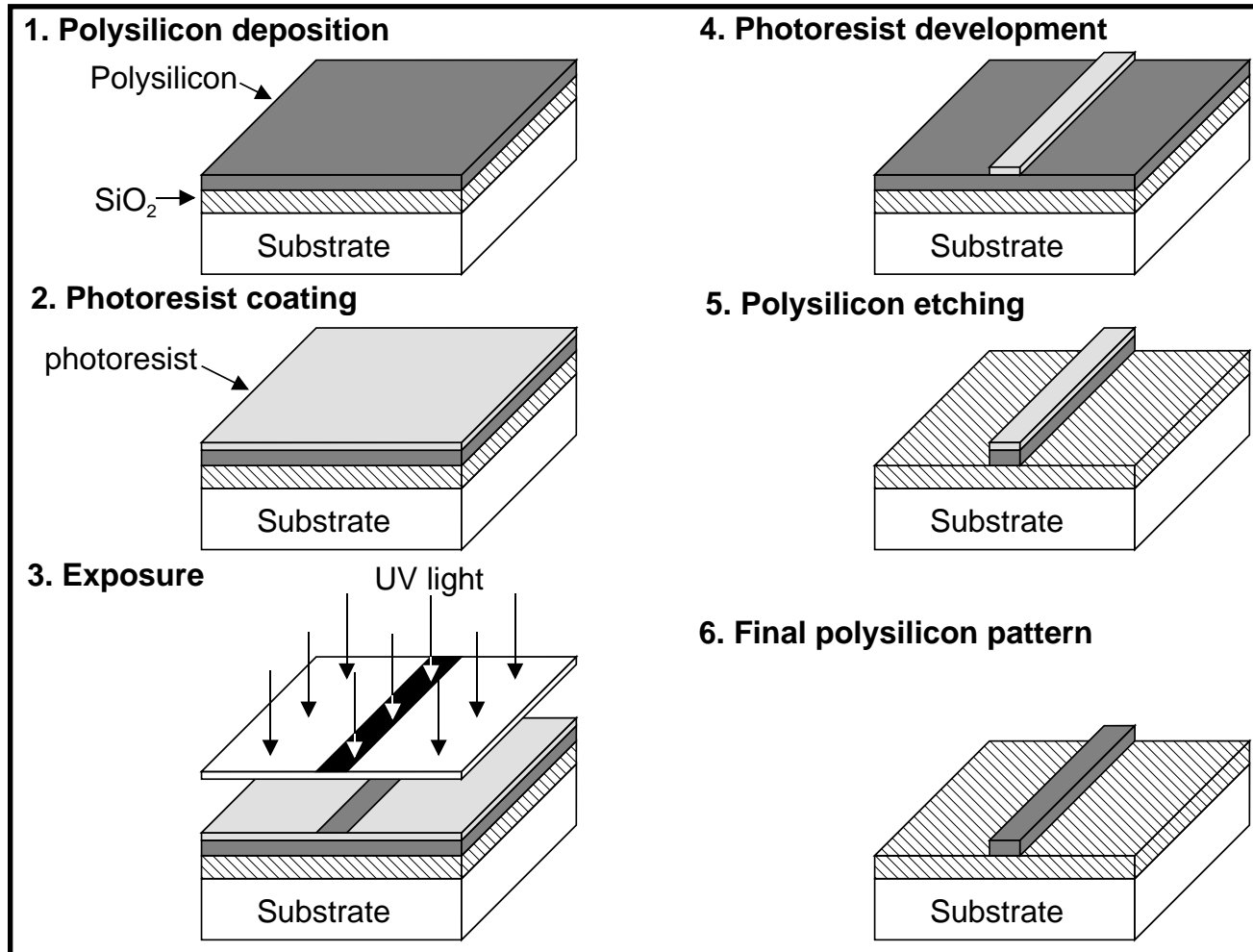
# Lithography

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- The lithographic sequence is repeated for each physical layer used to construct the IC. The sequence is always the same:
  - Photoresist application
  - Printing (exposure)
  - Development
  - Etching

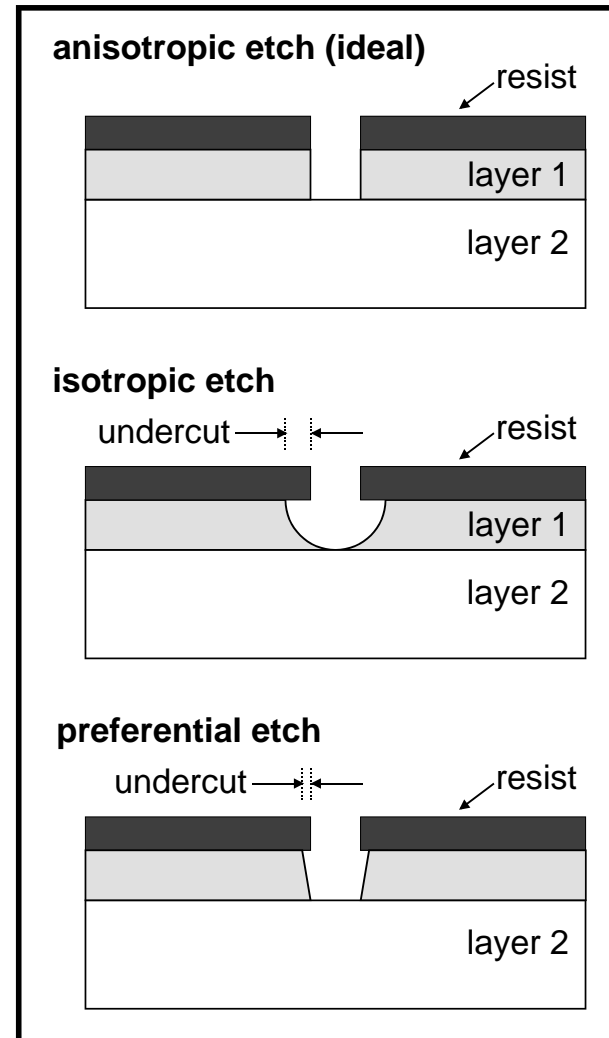
# Lithography

## Patterning a layer above the silicon surface

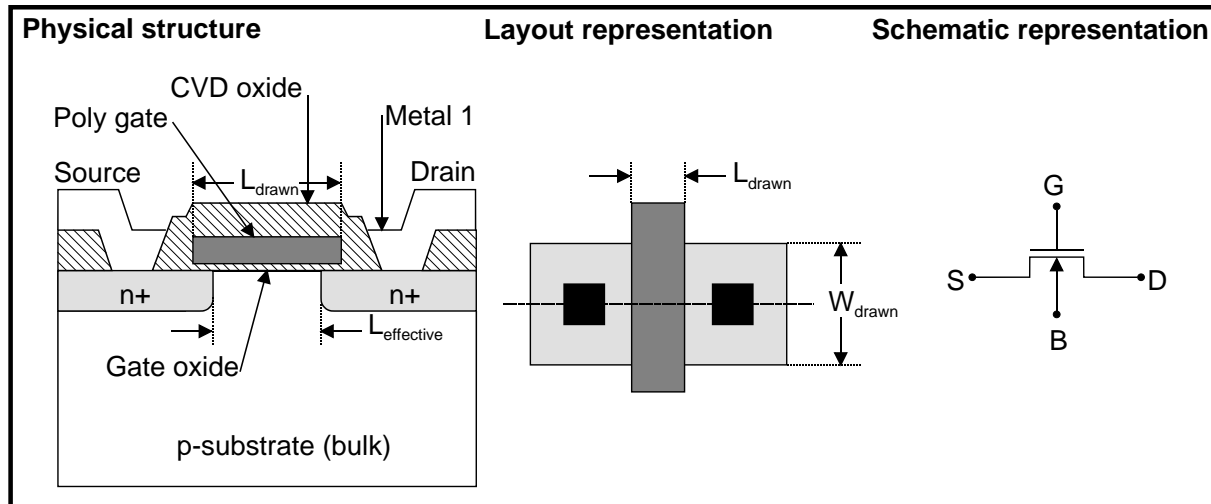


# Lithography

- **Etching:**
  - Process of removing unprotected material
  - Etching occurs in all directions
  - Horizontal etching causes an undercut
  - "preferential" etching can be used to minimize the undercut
- **Etching techniques:**
  - Wet etching: uses chemicals to remove the unprotected materials
  - Dry or plasma etching: uses ionized gases rendered chemically active by an rf-generated plasma



# Physical structure



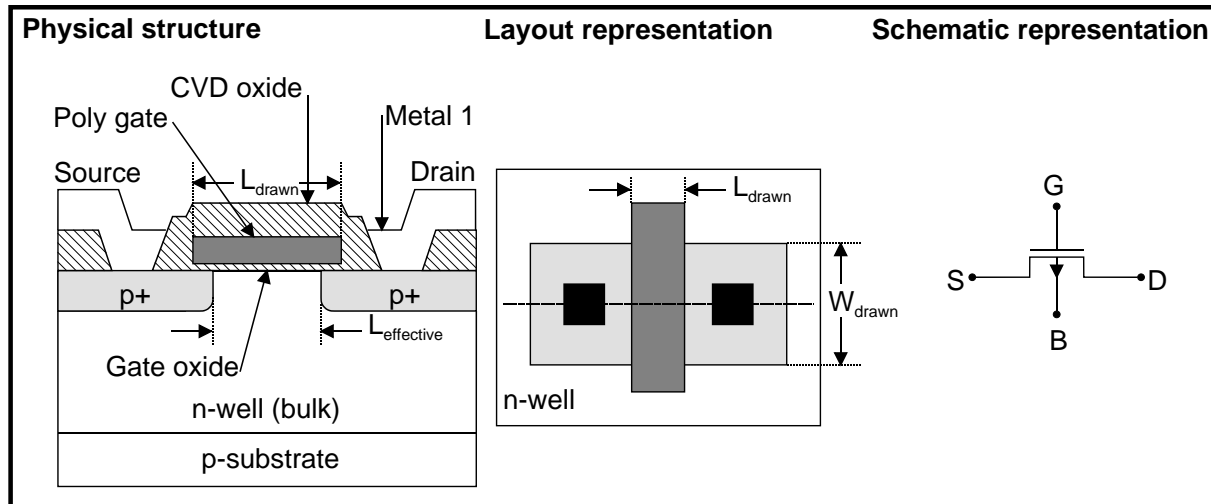
## NMOS physical structure:

- p-substrate
- n+ source/drain
- gate oxide ( $\text{SiO}_2$ )
- polysilicon gate
- CVD oxide
- metal 1
- $L_{\text{eff}} < L_{\text{drawn}}$  (lateral doping effects)

## NMOS layout representation:

- **Implicit layers:**
  - oxide layers
  - substrate (bulk)
- **Drawn layers:**
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

# Physical structure



## PMOS physical structure:

- p-substrate
- n-well (bulk)
- p+ source/drain
- gate oxide ( $\text{SiO}_2$ )
- polysilicon gate
- CVD oxide
- metal 1

## PMOS layout representation:

- **Implicit layers:**
  - oxide layers
- **Drawn layers:**
  - n-well (bulk)
  - n+ regions
  - polysilicon gate
  - oxide contact cuts
  - metal layers

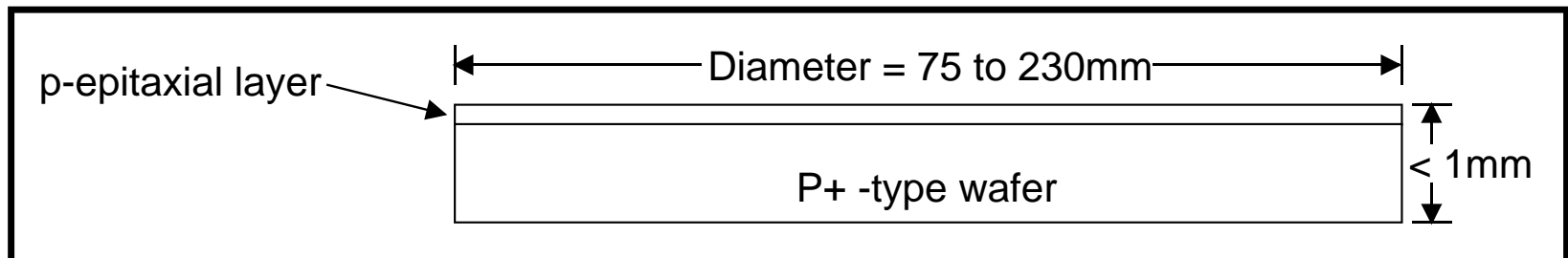
# CMOS fabrication sequence

## 0. Start:

- For an n-well process the starting point is a p-type silicon wafer:
- wafer: typically 75 to 230mm in diameter and less than 1mm thick

## 1. Epitaxial growth:

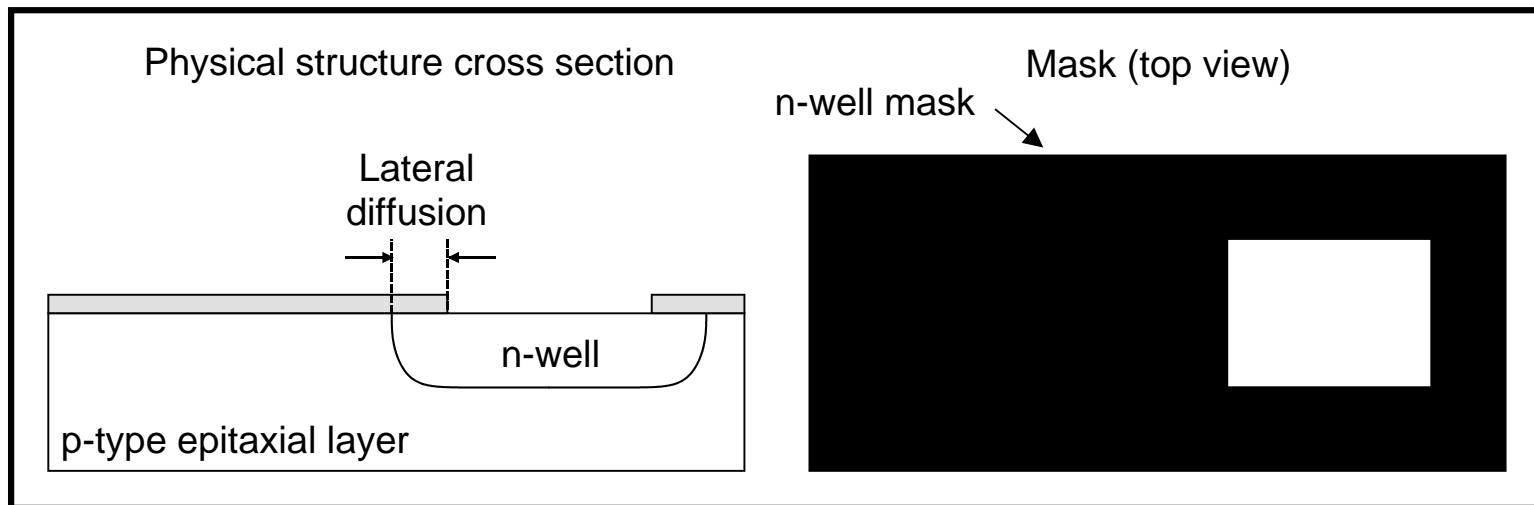
- A single p-type single crystal film is grown on the surface of the wafer by:
  - **subjecting the wafer to high temperature and a source of dopant material**
- The epi layer is used as the base layer to build the devices



# CMOS fabrication sequence

## 2. N-well Formation:

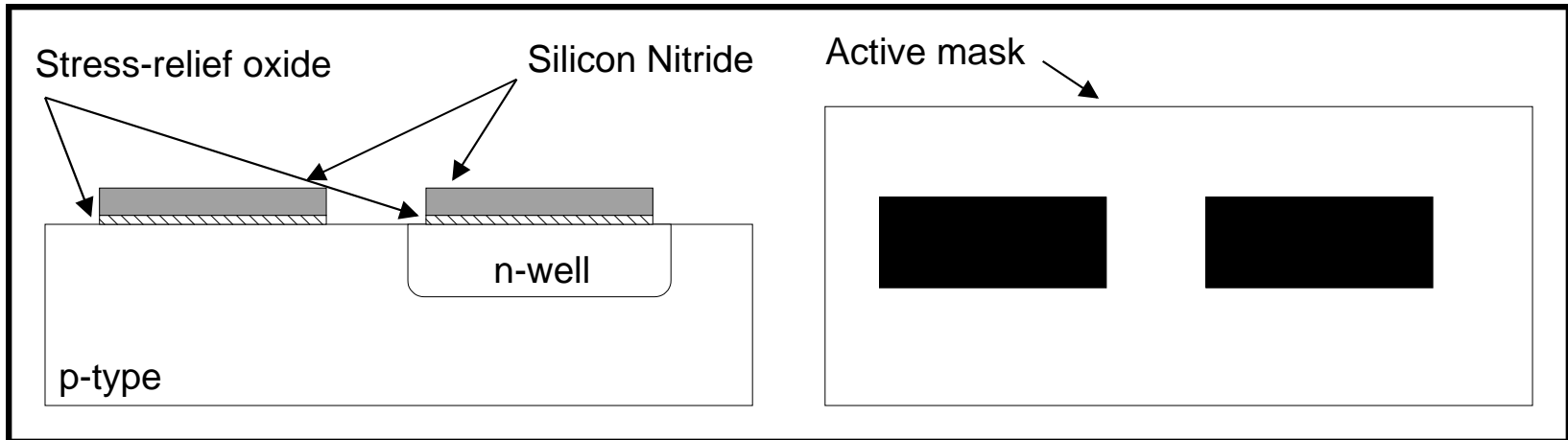
- PMOS transistors are fabricated in n-well regions
- The first mask defines the n-well regions
- N-wells are formed by ion implantation or deposition and diffusion
- Lateral diffusion limits the proximity between structures
- Ion implantation results in shallower wells compatible with today's fine-line processes



# CMOS fabrication sequence

## 3. Active area definition:

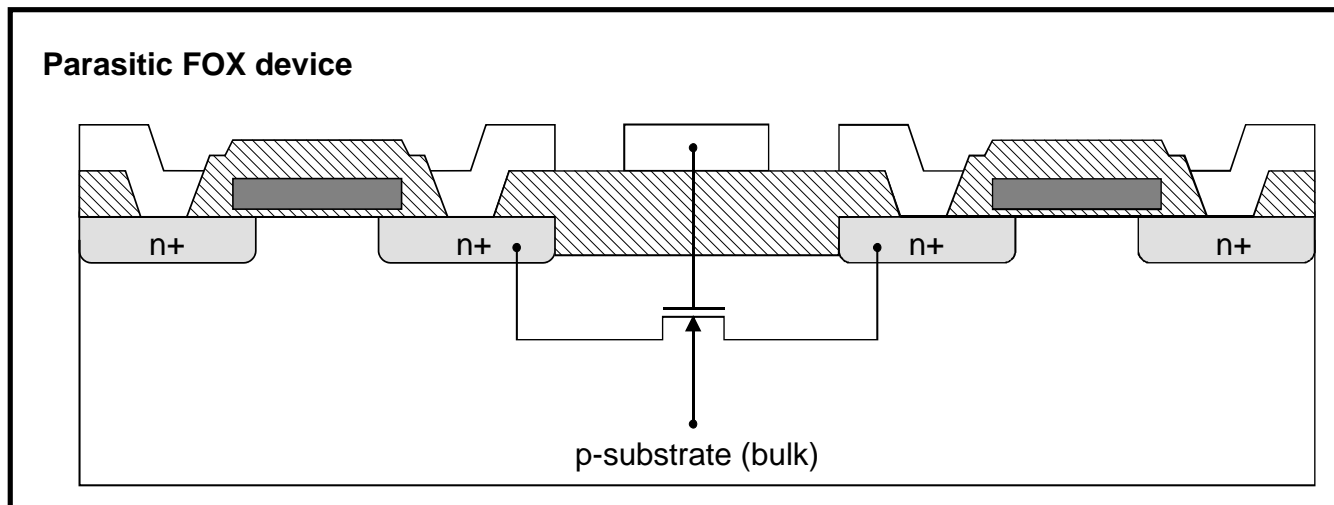
- Active area:
  - planar section of the surface where transistors are build
  - defines the gate region (thin oxide)
  - defines the n+ or p+ regions
- A thin layer of  $\text{SiO}_2$  is grown over the active region and covered with silicon nitride



# CMOS fabrication sequence

## 4. Isolation:

- Parasitic (unwanted) FET's exist between unrelated transistors (Field Oxide FET's)
- Source and drains are existing source and drains of wanted devices
- Gates are metal and polysilicon interconnects
- The threshold voltage of FOX FET's are higher than for normal FET's

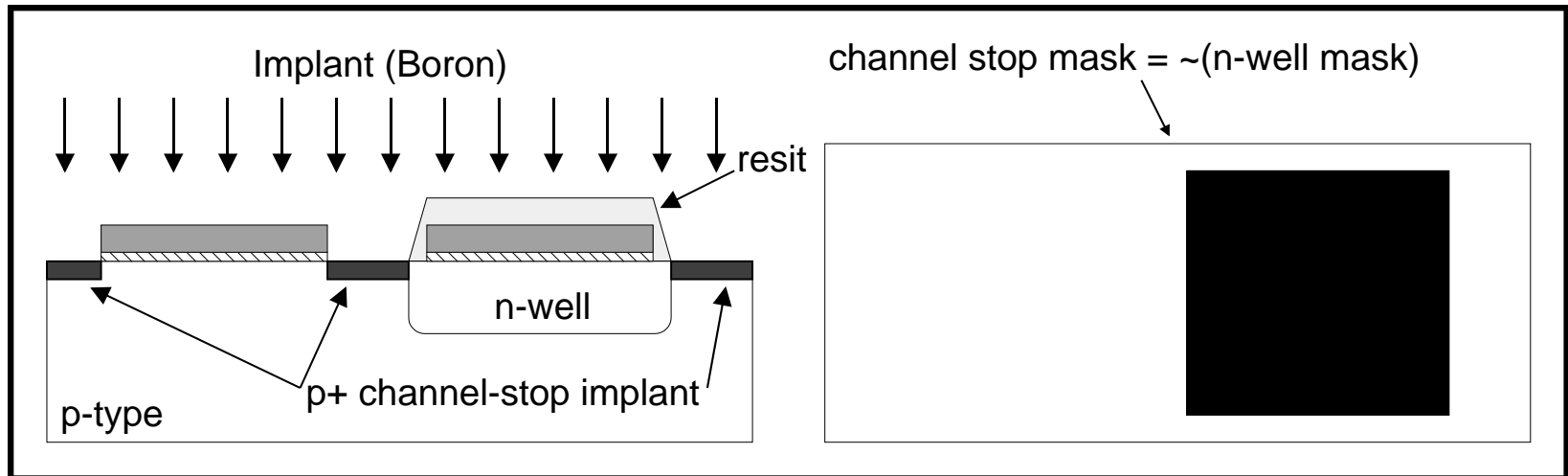


# CMOS fabrication sequence

- FOX FET's threshold is made high by:
  - introducing a channel-stop diffusion that raises the impurity concentration in the substrate in areas where transistors are not required
  - making the FOX thick

## 4.1 Channel-stop implant

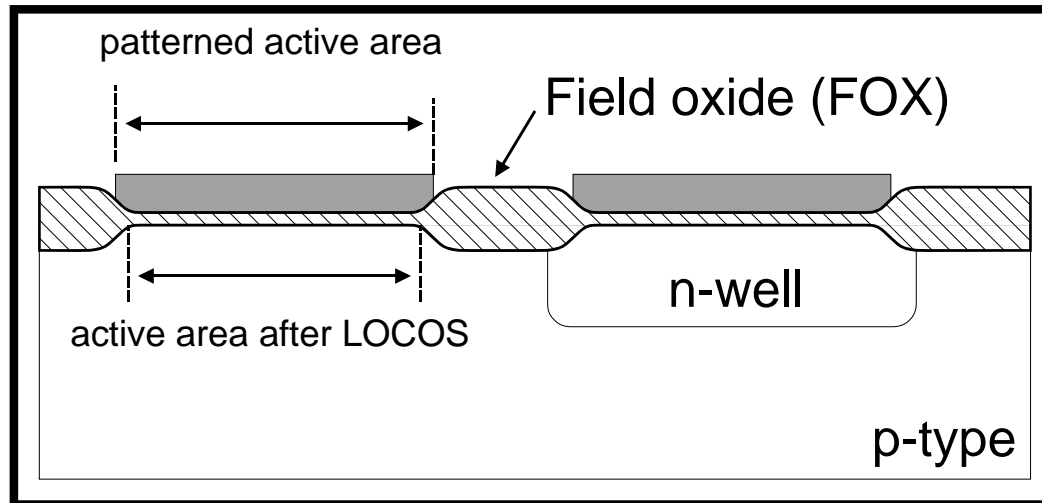
- The silicon nitride (over n-active) and the photoresist (over n-well) act as masks for the channel-stop implant



# CMOS fabrication sequence

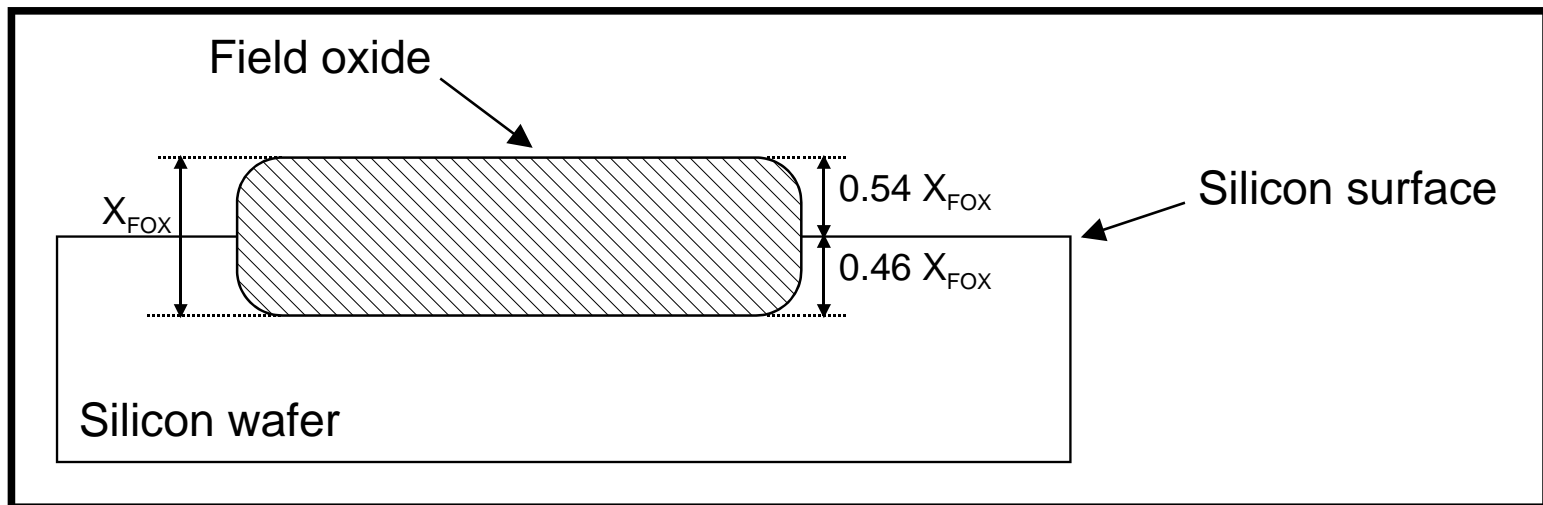
## 4.2 Local oxidation of silicon (LOCOS)

- The photoresist mask is removed
- The  $\text{SiO}_2/\text{SiN}$  layers will now act as a masks
- The thick field oxide is then grown by:
  - exposing the surface of the wafer to a flow of oxygen-rich gas
- The oxide grows in both the vertical and lateral directions
- This results in a active area smaller than patterned



# CMOS fabrication sequence

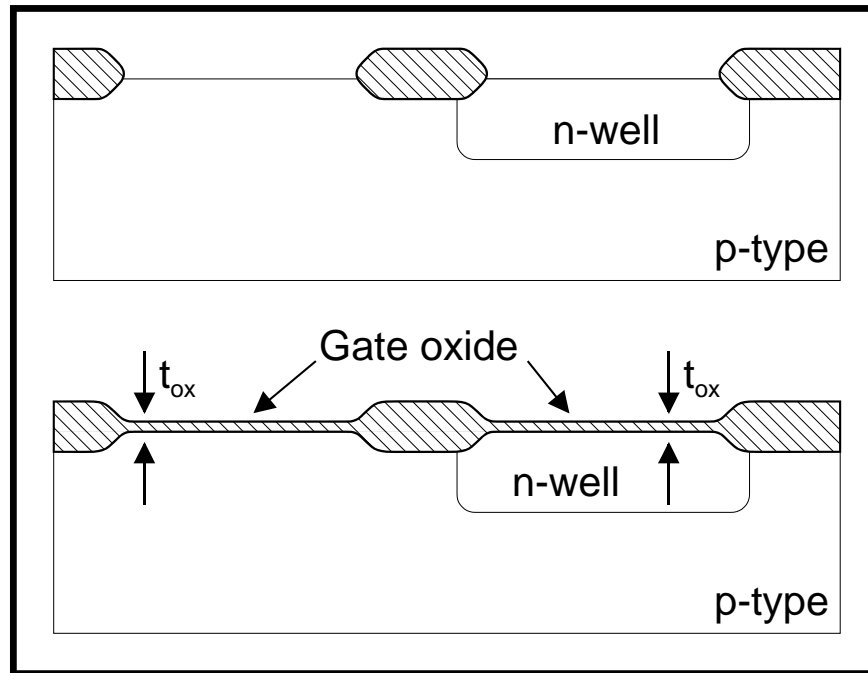
- Silicon oxidation is obtained by:
  - Heating the wafer in a oxidizing atmosphere:
    - Wet oxidation: water vapor,  $T = 900$  to  $1000^{\circ}\text{C}$  (rapid process)
    - Dry oxidation: Pure oxygen,  $T = 1200^{\circ}\text{C}$  (high temperature required to achieve an acceptable growth rate)
- Oxidation consumes silicon
  - $\text{SiO}_2$  has approximately twice the volume of silicon
  - The FOX is recedes below the silicon surface by  $0.46X_{\text{FOX}}$



# CMOS fabrication sequence

## 5. Gate oxide growth

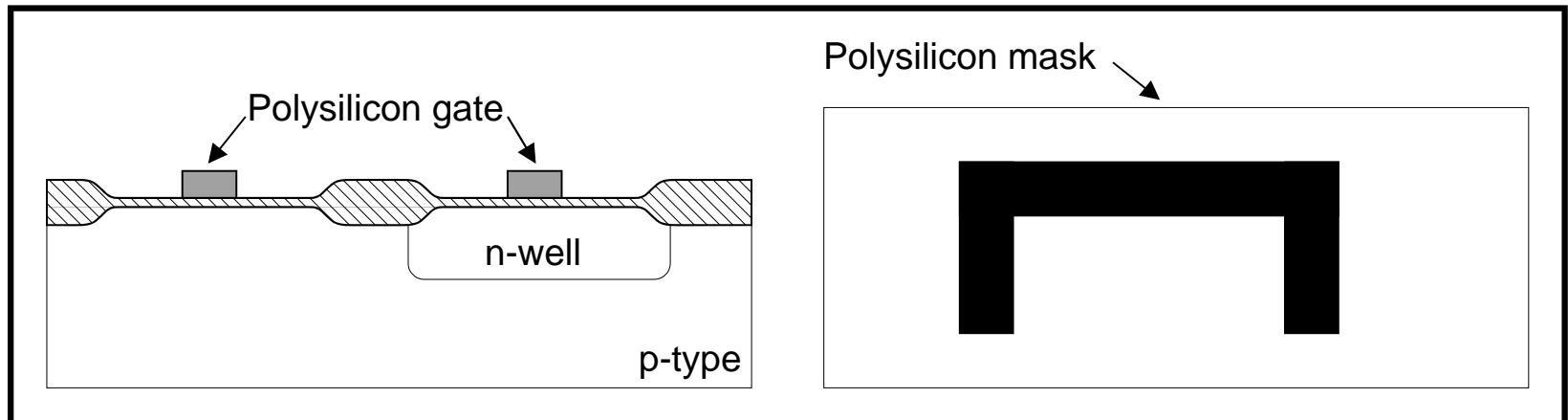
- The nitride and stress-relief oxide are removed
- The devices threshold voltage is adjusted by:
  - adding charge at the silicon/oxide interface
- The well controlled gate oxide is grown with thickness  $t_{ox}$



# CMOS fabrication sequence

## 6. Polysilicon deposition and patterning

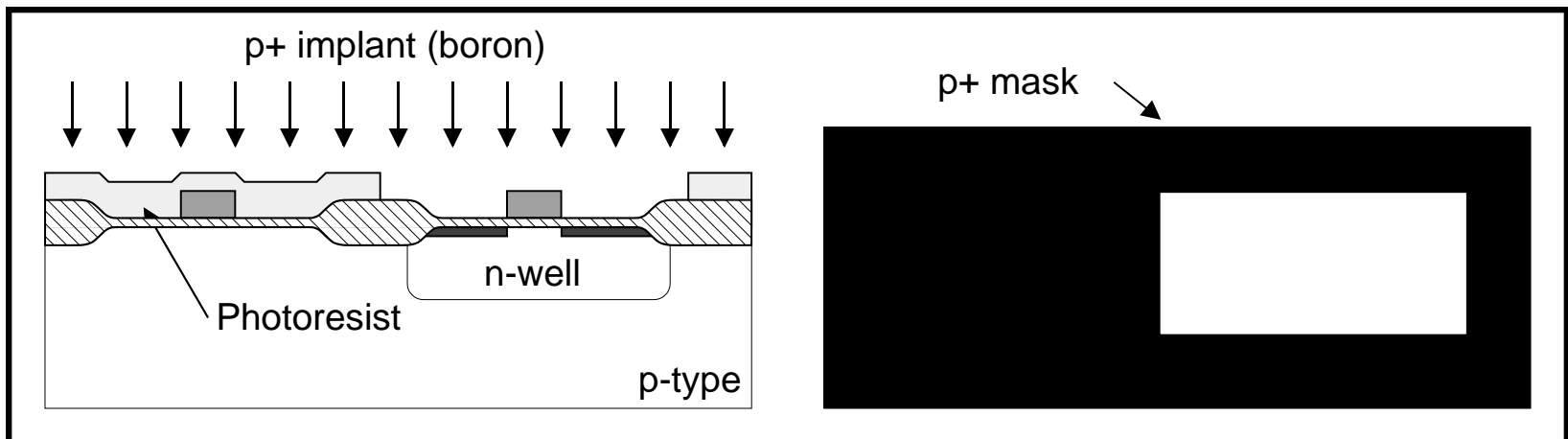
- A layer of polysilicon is deposited over the entire wafer surface
- The polysilicon is then patterned by a lithography sequence
- All the MOSFET gates are defined in a single step
- The polysilicon gate can be doped (n+) while is being deposited to lower its parasitic resistance (important in high speed fine line processes)



# CMOS fabrication sequence

## 7. PMOS formation

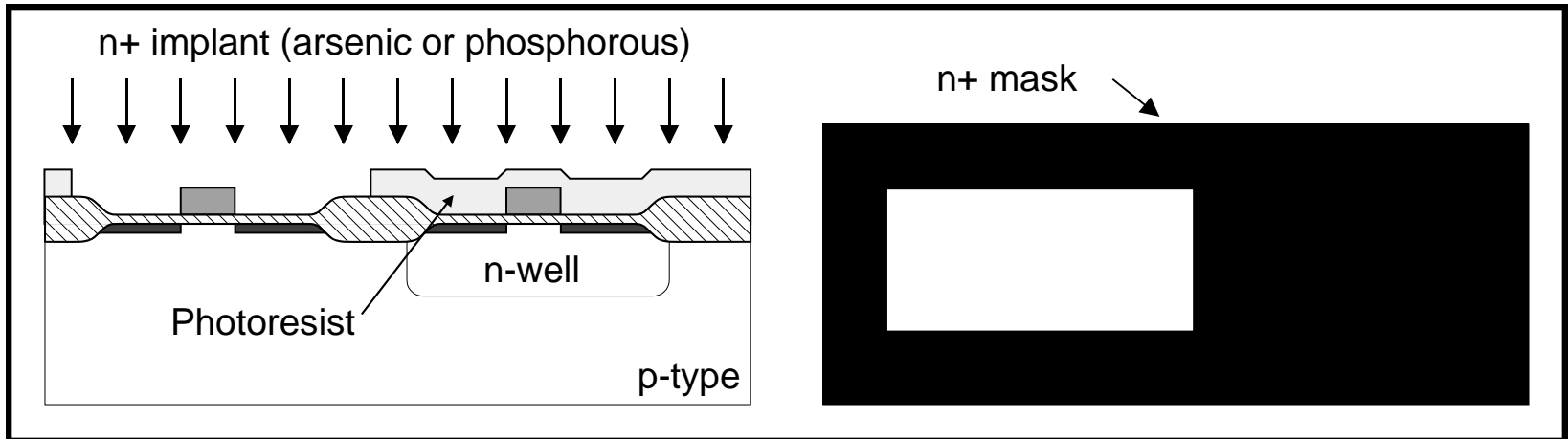
- Photoresist is patterned to cover all but the p+ regions
- A boron ion beam creates the p+ source and drain regions
- The polysilicon serves as a mask to the underlying channel
  - This is called a self-aligned process
  - It allows precise placement of the source and drain regions
- During this process the gate gets doped with p-type impurities
  - Since the gate had been doped n-type during deposition, the final type (n or p) will depend on which dopant is dominant



# CMOS fabrication sequence

## 8. NMOS formation

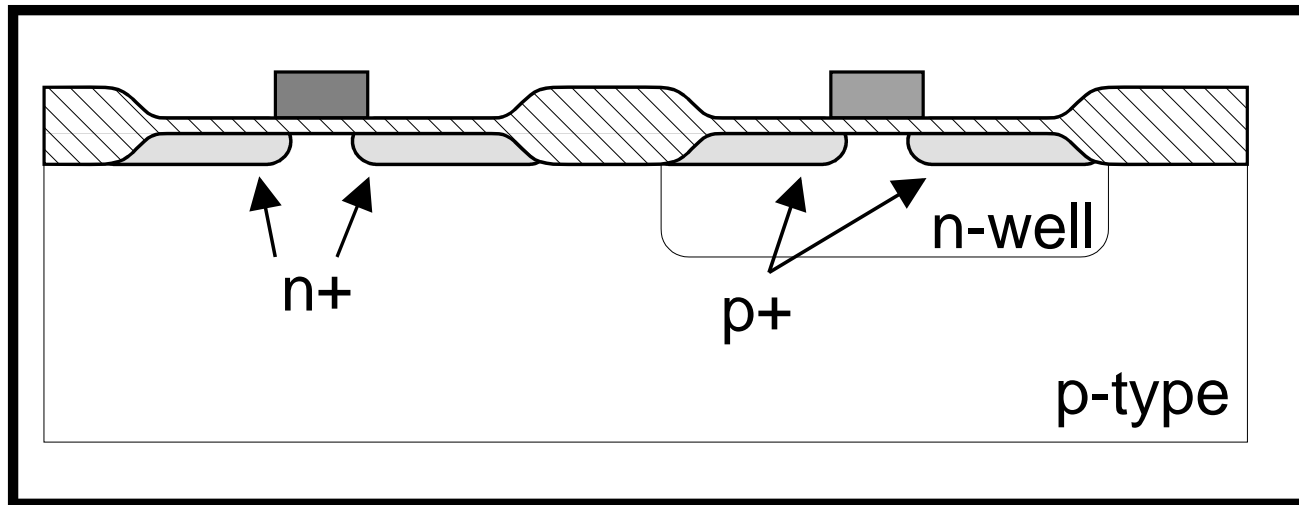
- Photoresist is patterned to define the n+ regions
- Donors (arsenic or phosphorous) are ion-implanted to dope the n+ source and drain regions
- The process is self-aligned
- The gate is n-type doped



# CMOS fabrication sequence

## 9. Annealing

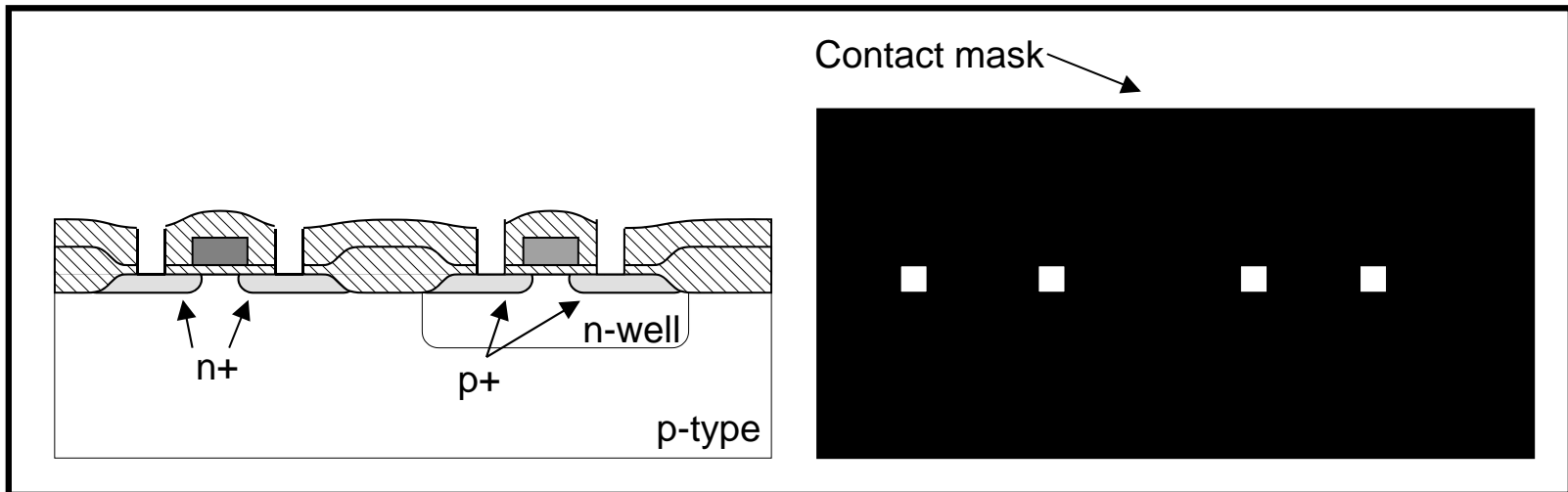
- After the implants are completed a thermal annealing cycle is executed
- This allows the impurities to diffuse further into the bulk
- After thermal annealing, it is important to keep the remaining process steps at as low temperature as possible



# CMOS fabrication sequence

## 10. Contact cuts

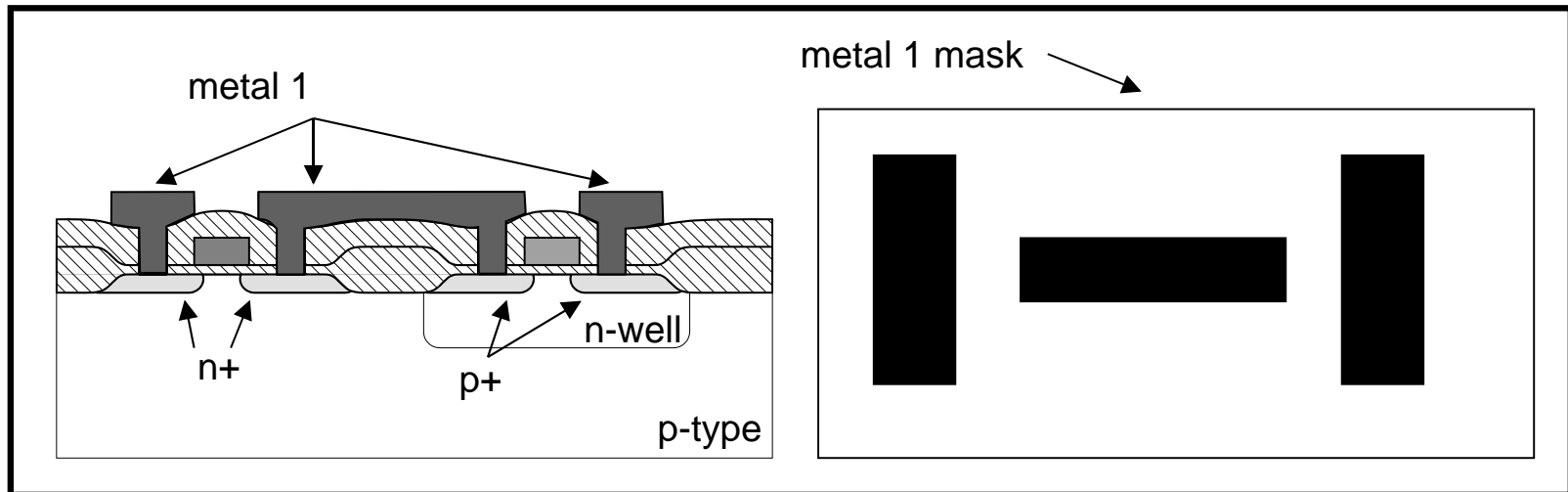
- The surface of the IC is covered by a layer of CVD oxide
  - The oxide is deposited at low temperature (LTO) to avoid that underlying doped regions will undergo diffusive spreading
- Contact cuts are defined by etching  $\text{SiO}_2$  down to the surface to be contacted
- These allow metal to contact diffusion and/or polysilicon regions



# CMOS fabrication sequence

## 11. Metal 1

- A first level of metallization is applied to the wafer surface and selectively etched to produce the interconnects





# CMOS fabrication sequence

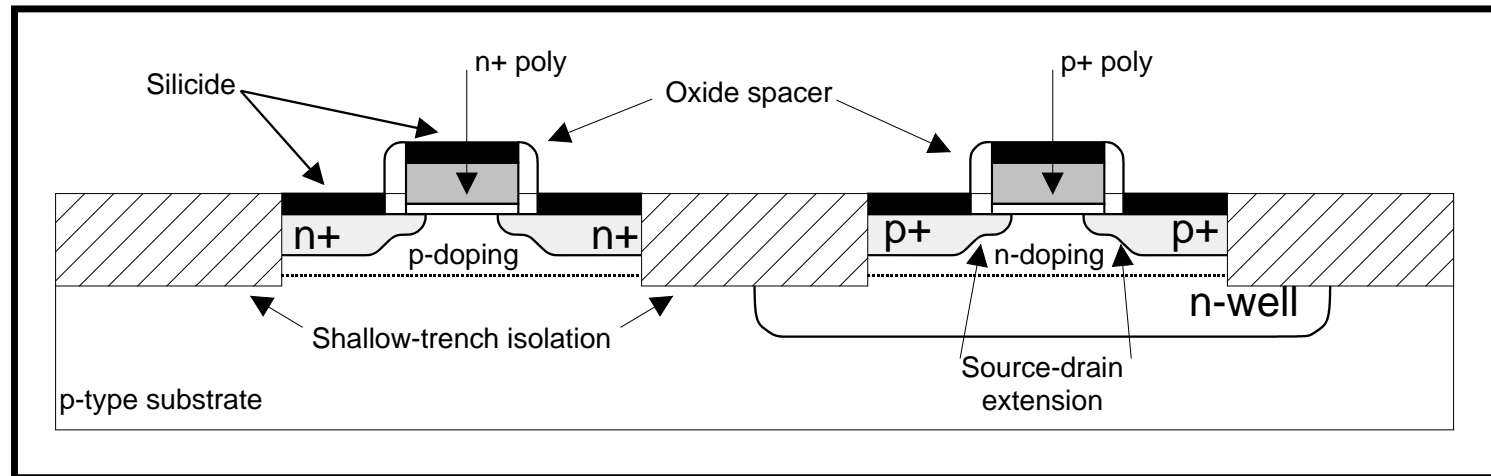
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## 13. Over glass and pad openings

- A protective layer is added over the surface:
- The protective layer consists of:
  - A layer of  $\text{SiO}_2$
  - Followed by a layer of silicon nitride
- The SiN layer acts as a diffusion barrier against contaminants (passivation)
- Finally, contact cuts are etched, over metal 2, on the passivation to allow for wire bonding.

# Advanced CMOS processes

- Shallow trench isolation
- n+ and p+-doped polysilicon gates (low threshold)
- source-drain extensions LDD (hot-electron effects)
- Self-aligned silicide (spacers)
- Non-uniform channel doping (short-channel effects)



# Process enhancements

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- Twin-well formation
- Copper interconnects
  - Up to 8 metal levels in modern processes
- Stacked contacts and vias
- Chemical Metal Polishing for technologies with several metal levels
- Shallow trench isolation
- Bipolar transistors (BiCMOS)
- Capacitors
- Diodes
- Inductors
- Resistors
- Dual or triple polysilicon (memories)
- Separate n-channel and p-channel implant