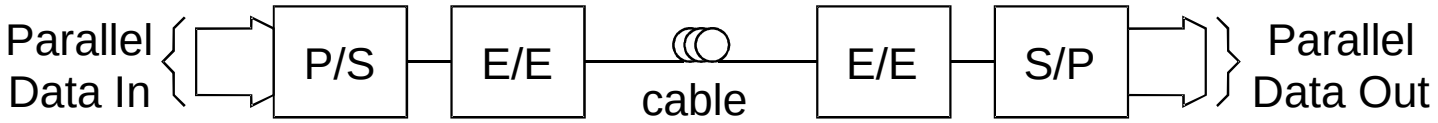
Functions and Circuits

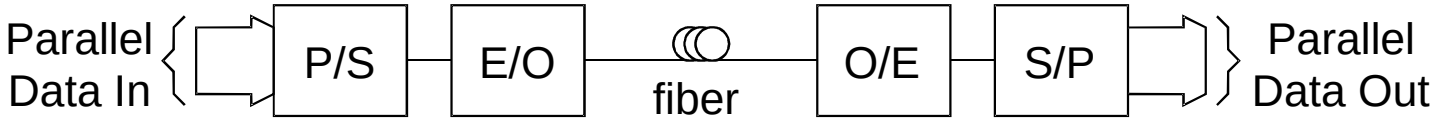
- Serial transmitters and receivers
  - Architecture
- Transmitters:
  - Parallel to serial converters
  - Clock generation circuits and PLL's
  - Coding
  - Lasers & laser drivers:
    - Lasers E/O characteristics
    - Driver circuits & Mean power control
- Optical receivers
  - PIN diodes
  - Fiber-optic receivers
  - Limiting and AGC amplifiers
  - Clock recovery circuits and PLL's

Serial Transmitters and Receivers

Electrical transmission link:



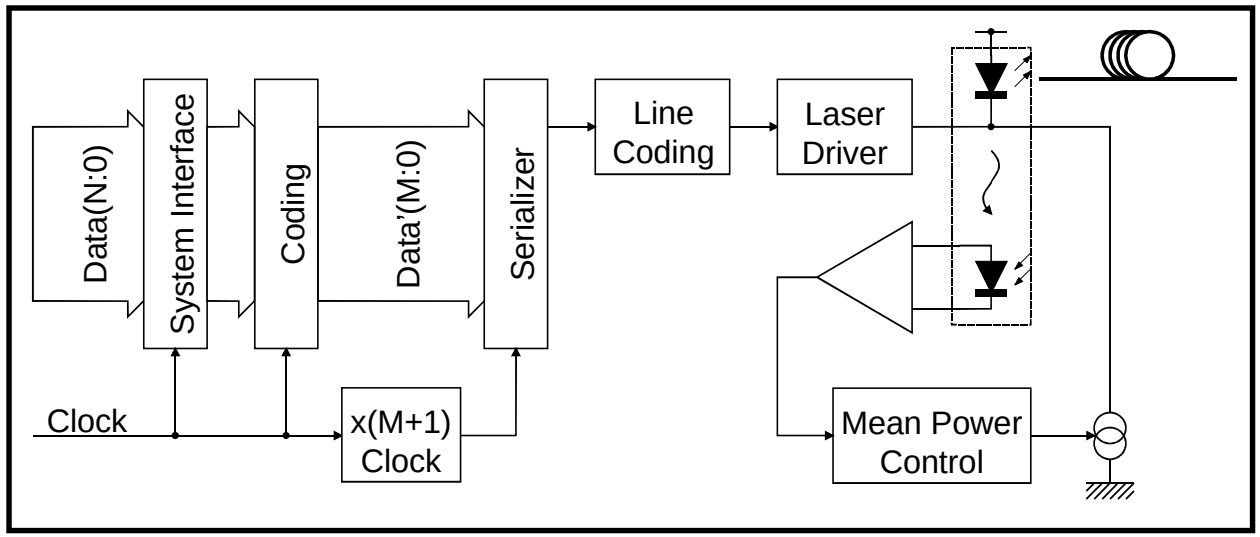
Lightwave transmission link:



Serial Link:

- P/S converter
- Transmitter
- Physical medium
- Receiver
- S/P converter

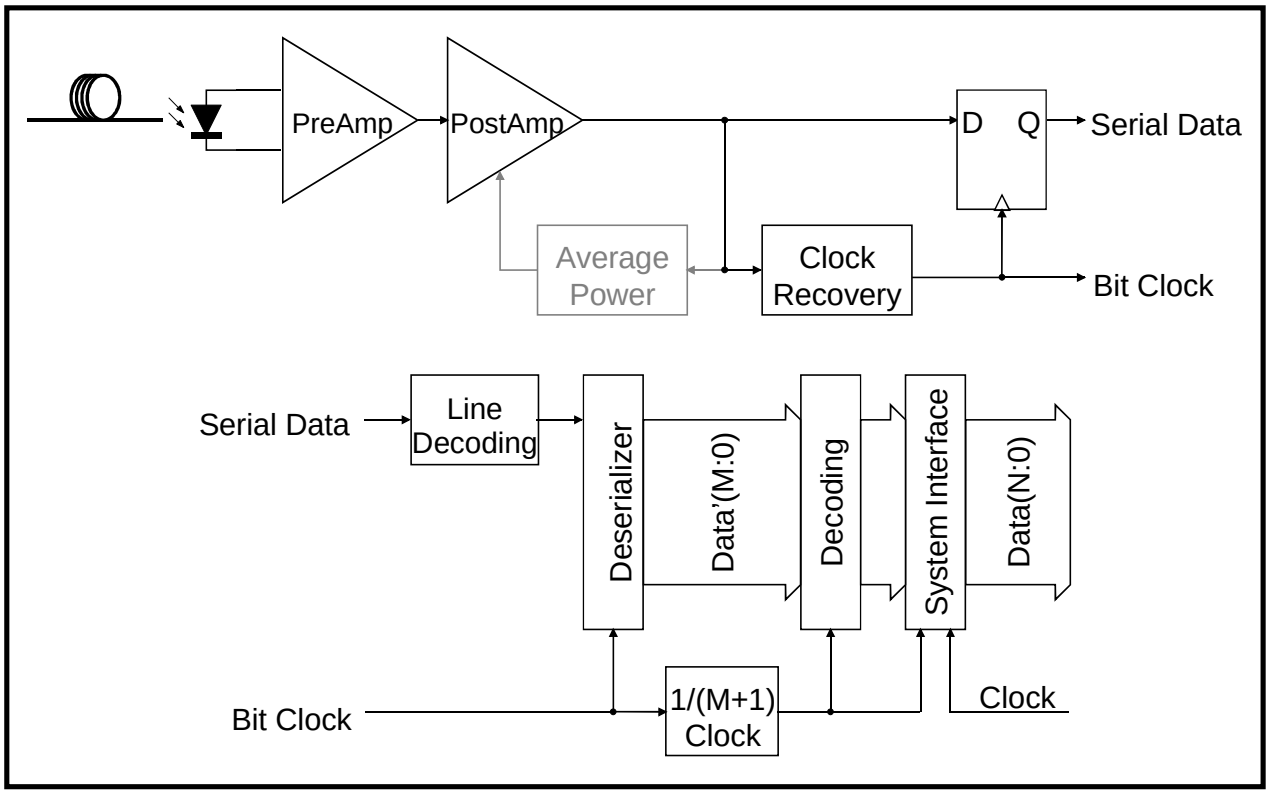
Transmitter Architecture



Main functions:

- System Interface:
  - Synchronization with the data source
- Coding:
  - Error control
  - Line coding
- Clock frequency multiplication
- Parallel-to-Serial conversion
- Electrical-to-Optical conversion
- Laser light mean power control

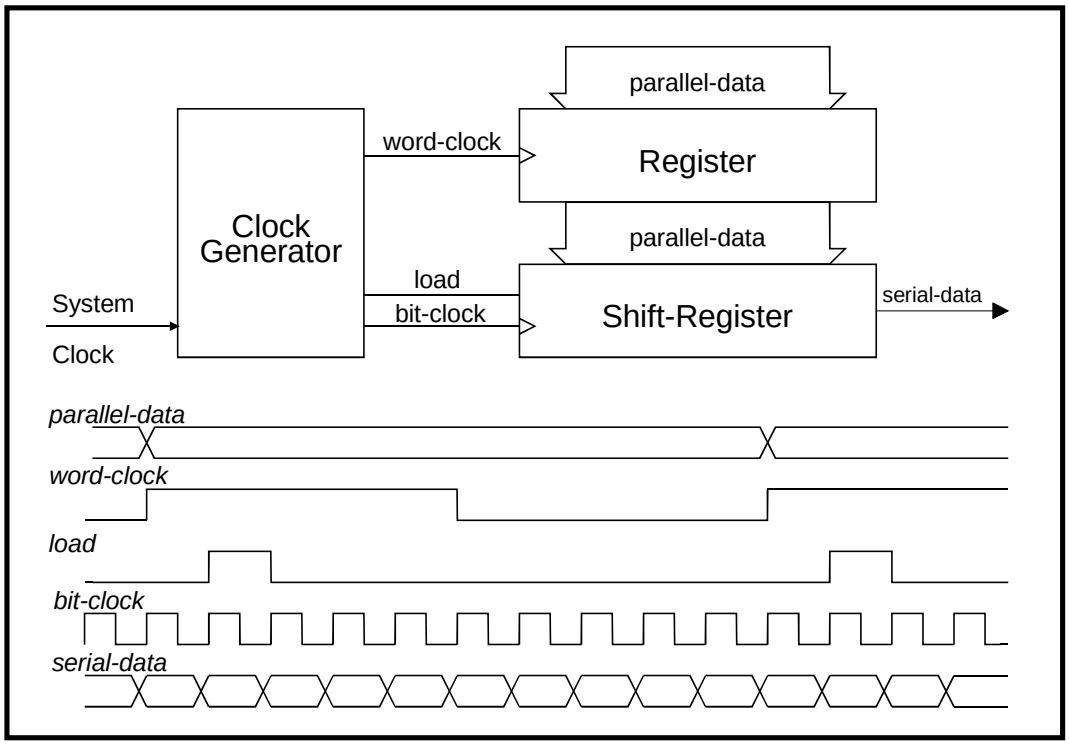
Receiver Architecture



Main Functions:

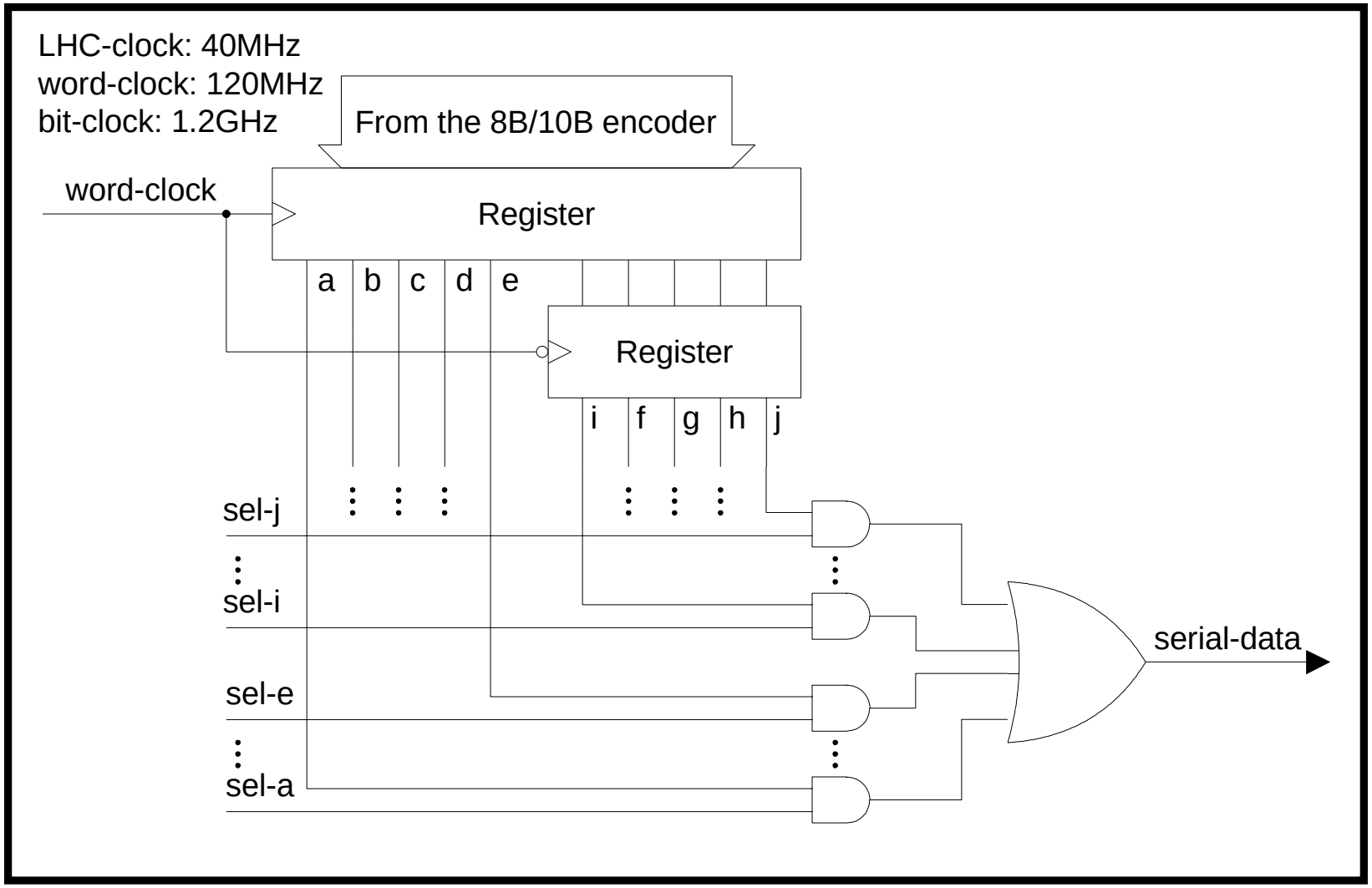
- Electrical-to-optical conversion
- Signal amplification
- Clock Recovery
- Binary decision
- Decoding:
  - Line decoding
  - Error detection and correction
- Serial-to-parallel conversion
- System interface
  - synchronization

Parallel to Serial Converters

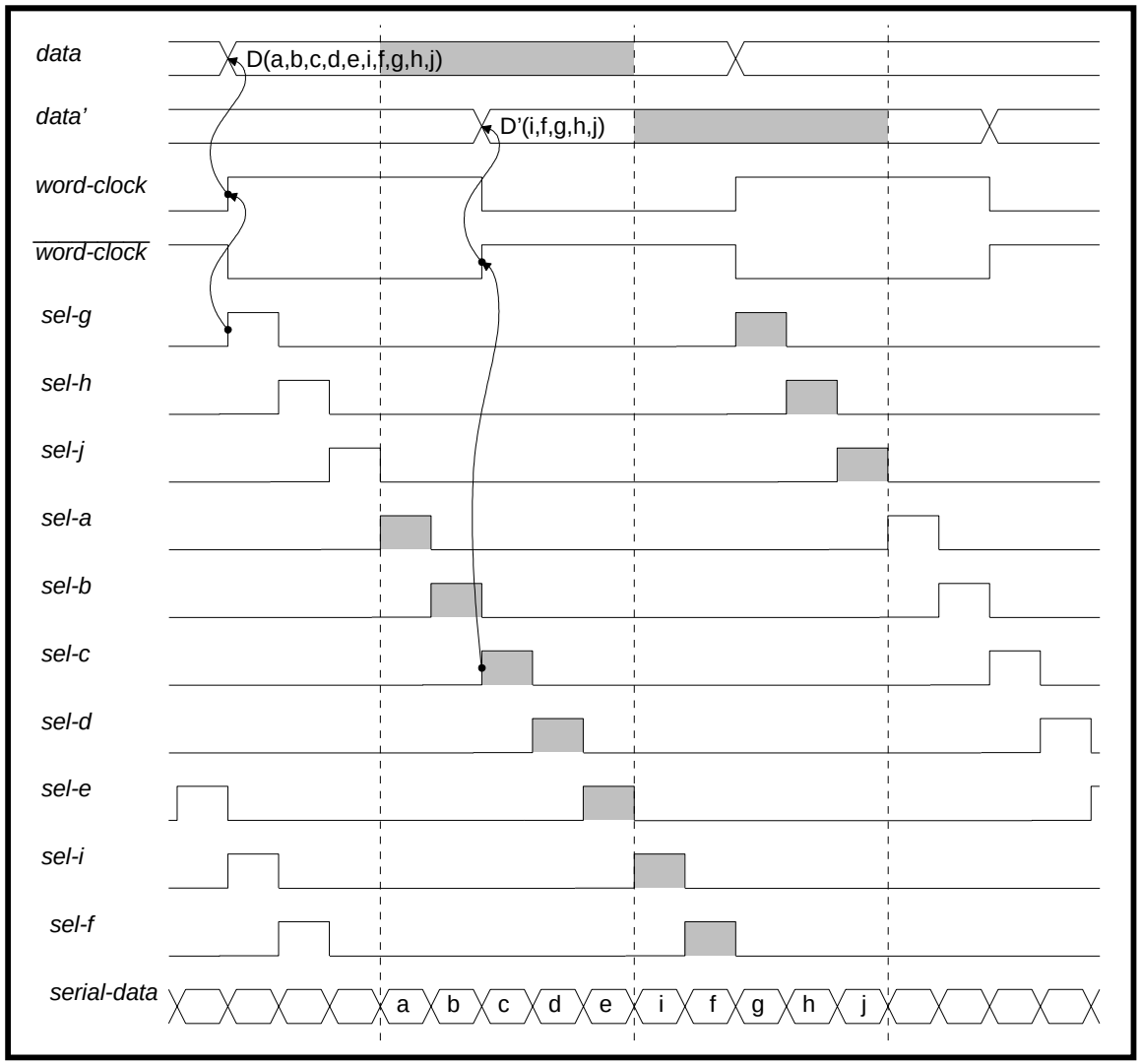


- The simplest possible serializer is a shift-register
- Technology “speed” limitations may require other types of implementations:
  - Multiplexer
  - Bit interleaving

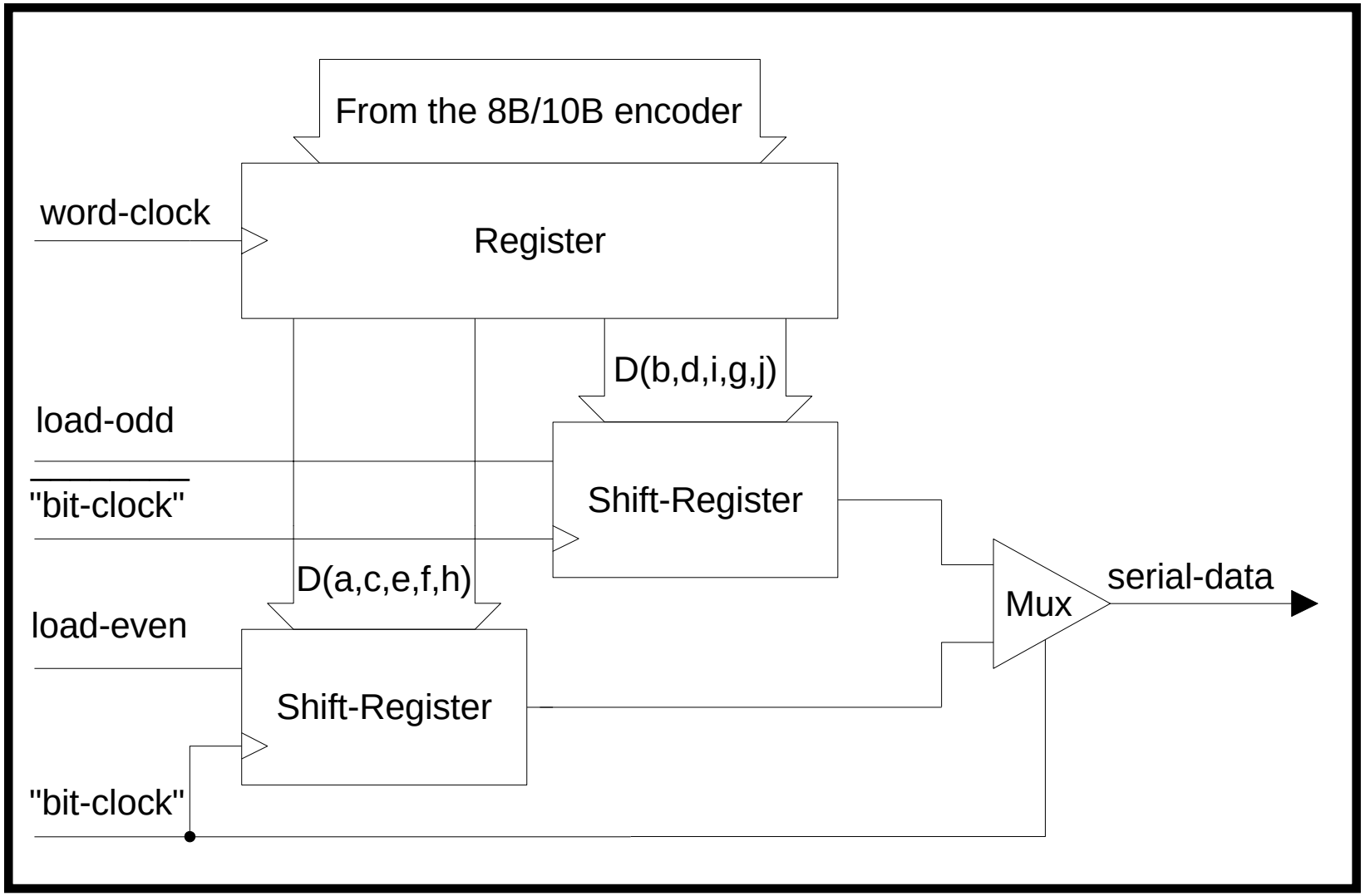
P/S Converter: Multiplexer



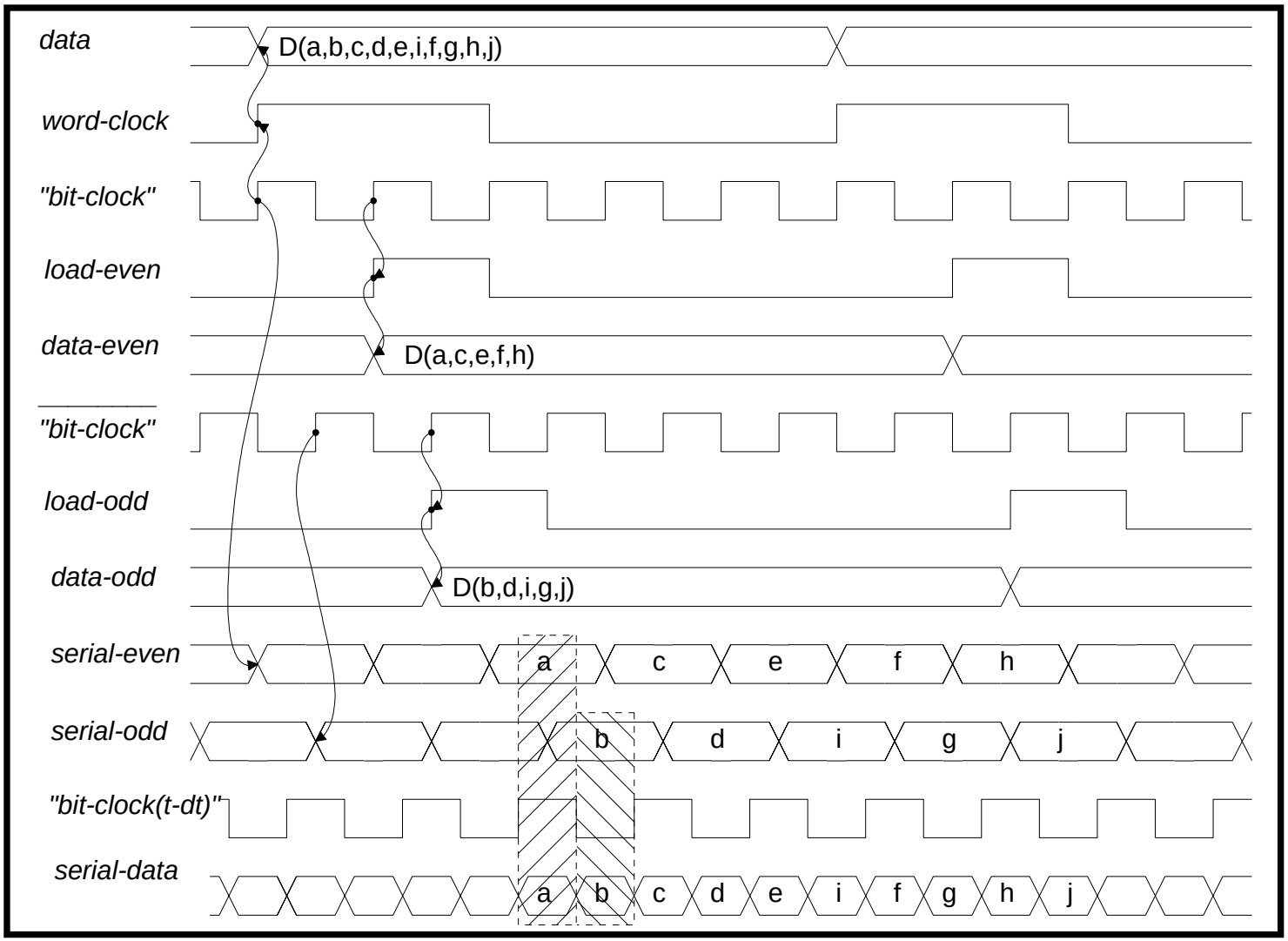
P/S Converter: Multiplexer



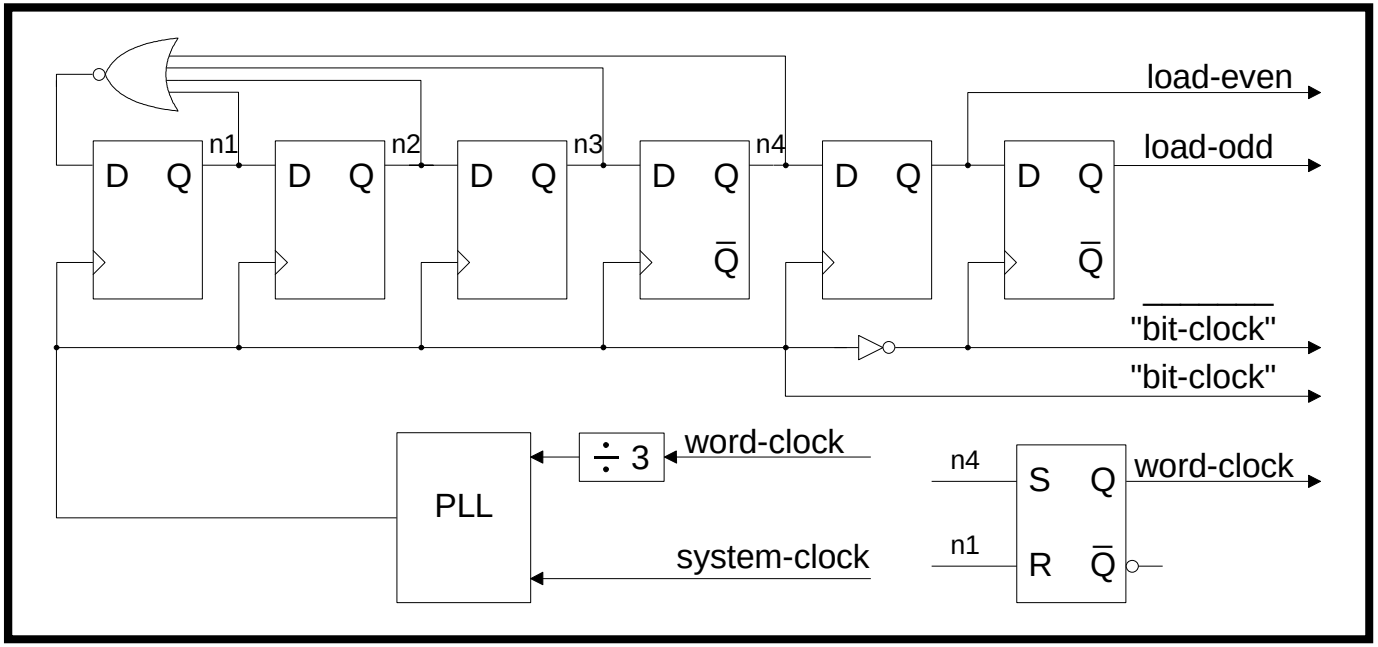
P/S Converter: Bit Interleaving



P/S Converter: Bit Interleaving

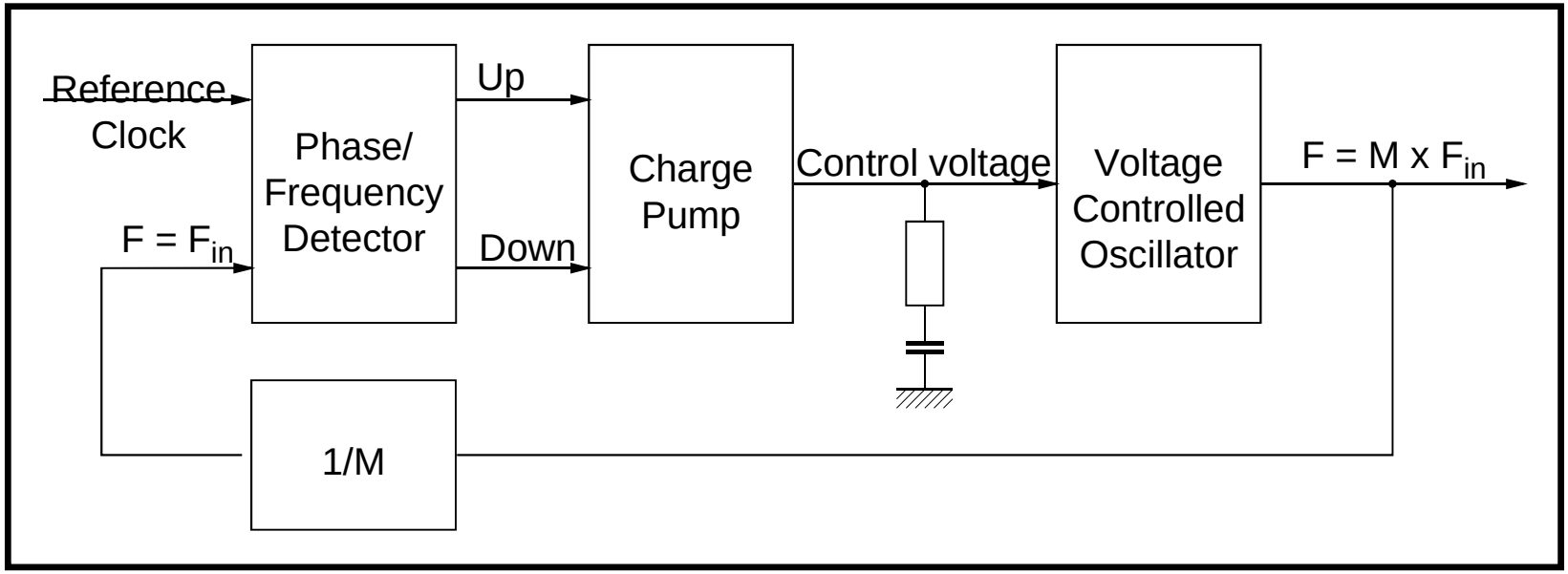


Clock Generation



- Necessary to generate the serializer control signals
- Required to obtain the “bit” clock:
  - From the system clock
  - From a local low frequency reference clock
- Clock multiplication can be implemented by:
  - A clock multiplying PLL
  - Combination of the multiple clock phases obtained from a DLL

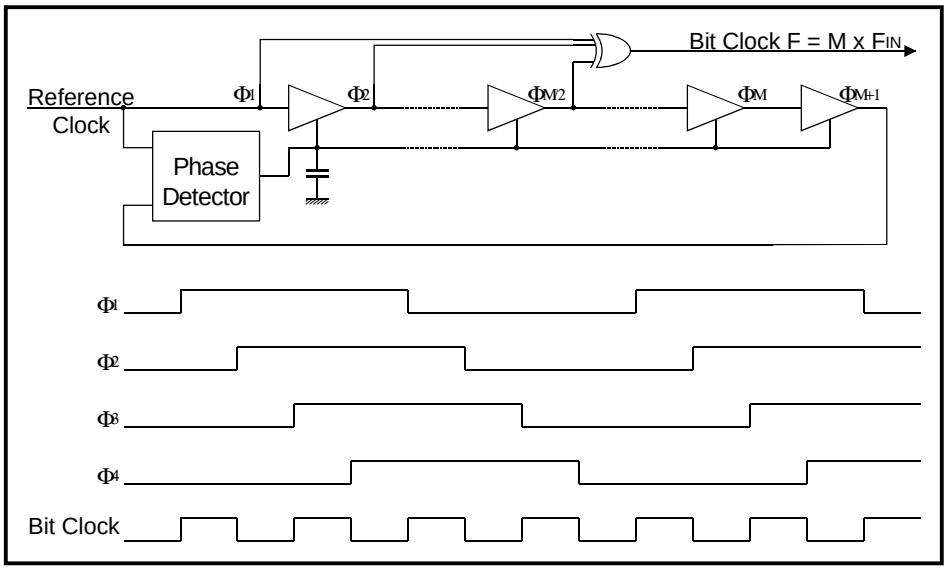
Clock Generation



Clock Multiplying PLL's:

- A PLL can be used to synthesize different clock frequencies from a reference clock
- The synthesized frequencies are phase locked to the reference signal
- Frequency up conversion is obtained by the divide by "1/M" block in the feedback loop
- PLL's can be used to reduce phase noise:
- "Hi" phase noise reference:
  - A low bandwidth PLL can be used to produce a low phase noise output
- Low phase noise reference:
  - A high bandwidth PLL can be used to reduce the PLL VCO noise

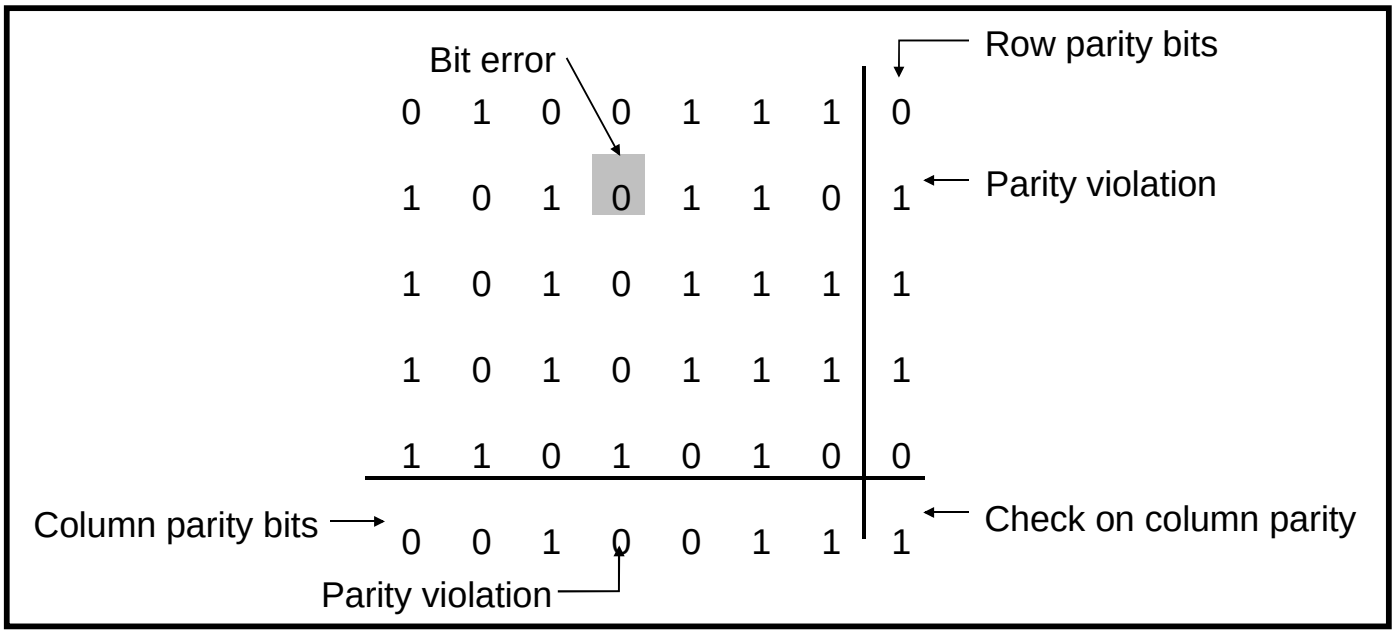
Clock Generation



DLL based clock generation:

- A high frequency clock can be obtained from the combination of multiple phases of a DLL
- A DLL has no phase noise filtering capability
  - The output phase noise is at best equal to the input signal phase noise
- Mismatch in the delay elements is converted into jitter in “clock multiplication” applications
- High multiplication factors are cumbersome to obtain
- However, DLL’s are easier to design than PLL’s

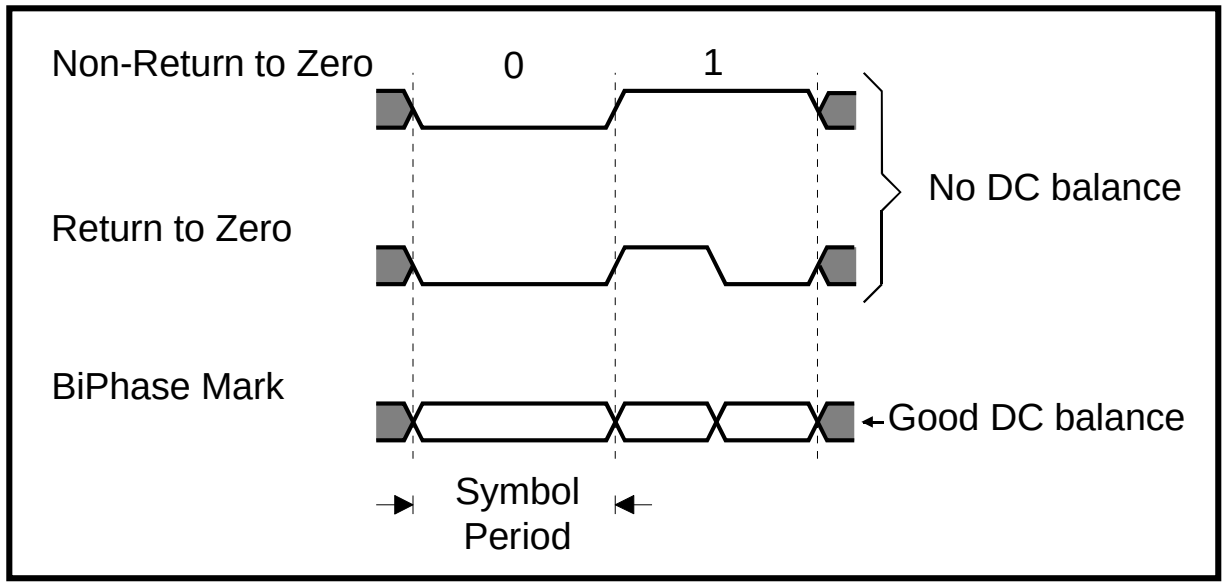
Coding: Error Control



Error control:

- Error detection:
  - Parity on single words
  - Check sum on multiple words
- Error detection and correction:
  - Row and column parity checks
  - Block coding: Ex. Hamming coding

Coding: Line Coding



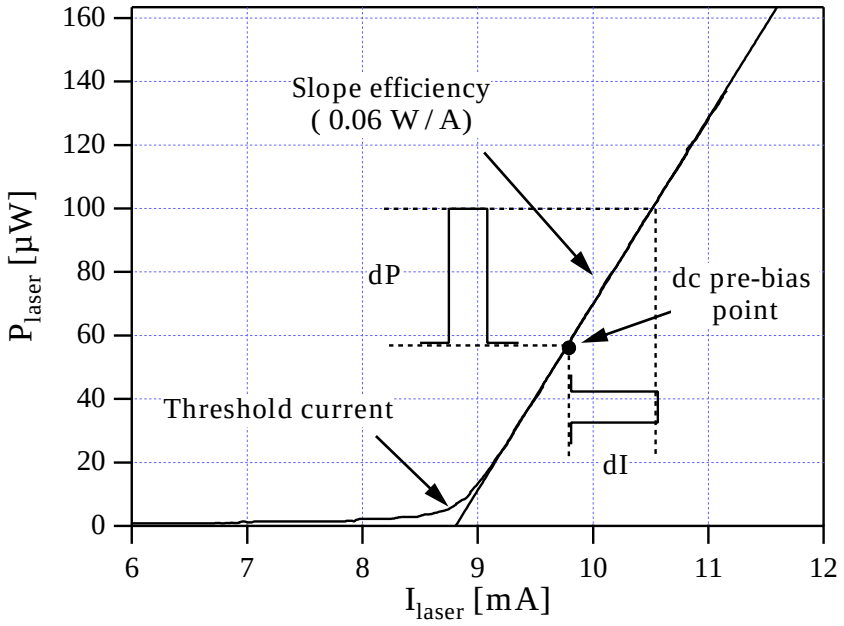
Line coding:

- Used to match the signal characteristics with those of the channel:
  - Limit the DC contents of the signal
  - Facilitate clock recovery
- Frequent used line codes are:
  - Return to zero
  - NRZI non-return to zero invert on ones
  - Manchester and Bi-Phase Mark
  - 3B/4B, 5B/6B and 8B/10B, done in groups of bits before serialization

Lasers & Laser Drivers

Laser E/O characteristics:

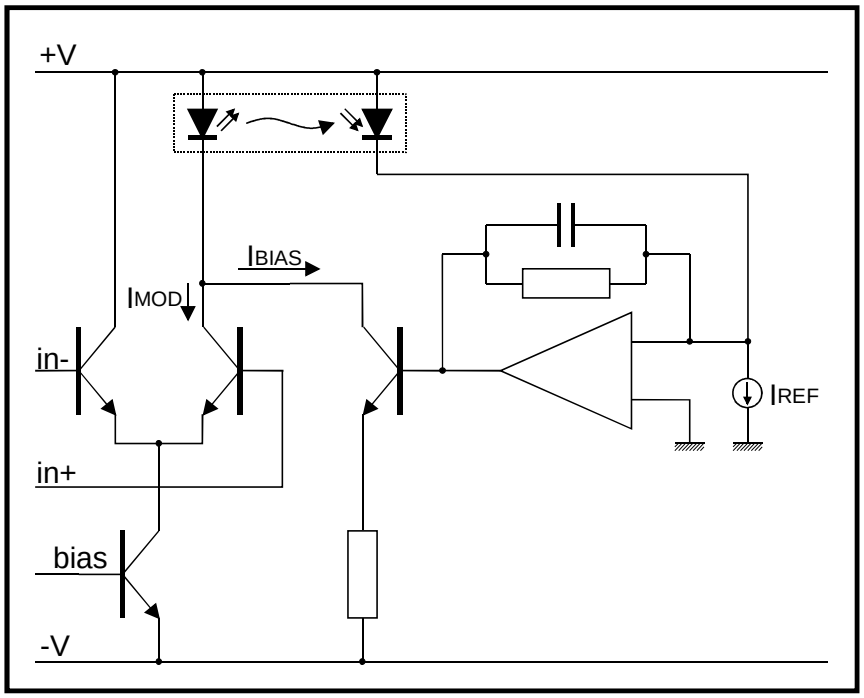
- Laser diodes are operated in the stimulated emission region
- This region happens above a given bias current called the threshold current I_{TH}
- Above threshold the optical power is roughly proportional to the modulation current
- I_{TH} increases with temperature: to avoid possible loss of laser operation, control of the mean optical power is done in the transmitter



Lasers & Laser Drivers

Laser Driver:

- The laser driver converts the input signal into a modulation current
- The modulation current is added to the pre-bias current
- The mean optical power emitted by the laser diode is measured by an optical feedback network
- The feedback network controls the pre-bias current in order to maintain the laser operation in the stimulated emission region

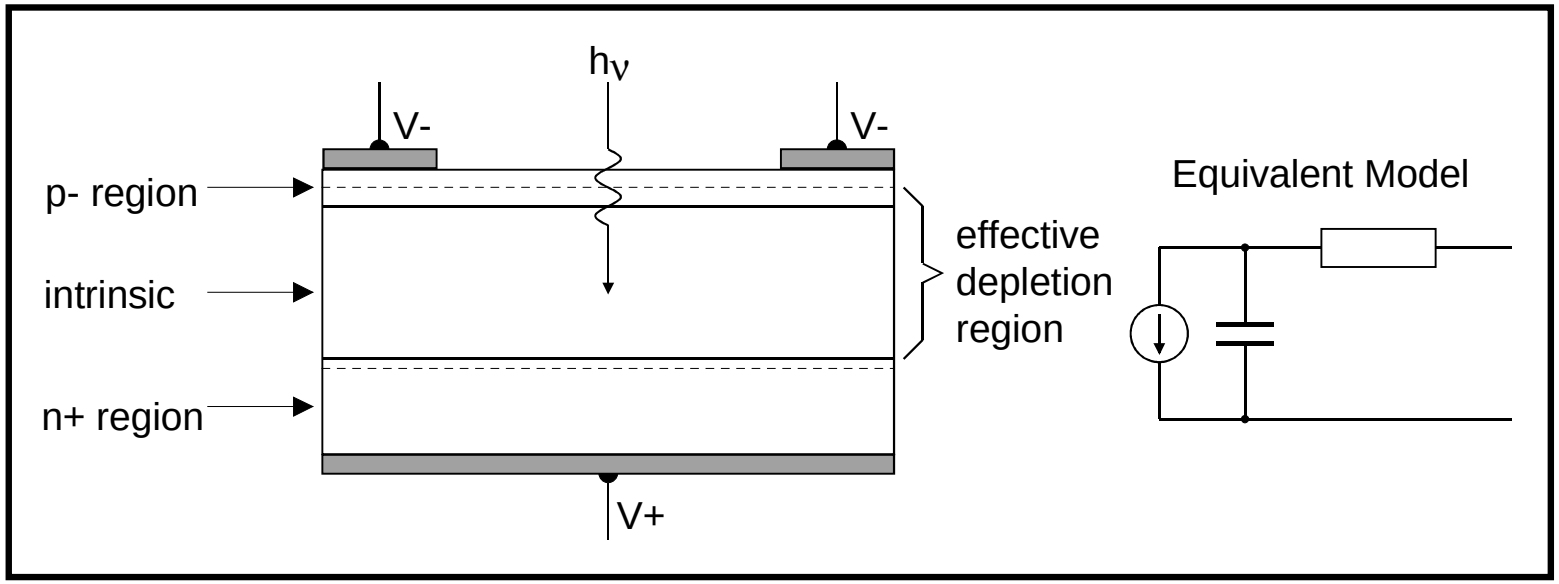


PIN Diodes

- A PIN diode converts the detected light into a current:

$$I_{ph} = \eta \cdot \frac{q\lambda}{hc} \cdot P_{opt}$$

- Its most important characteristics are:
  - The quantum efficiency η
  - The equivalent capacitance
  - The dark current

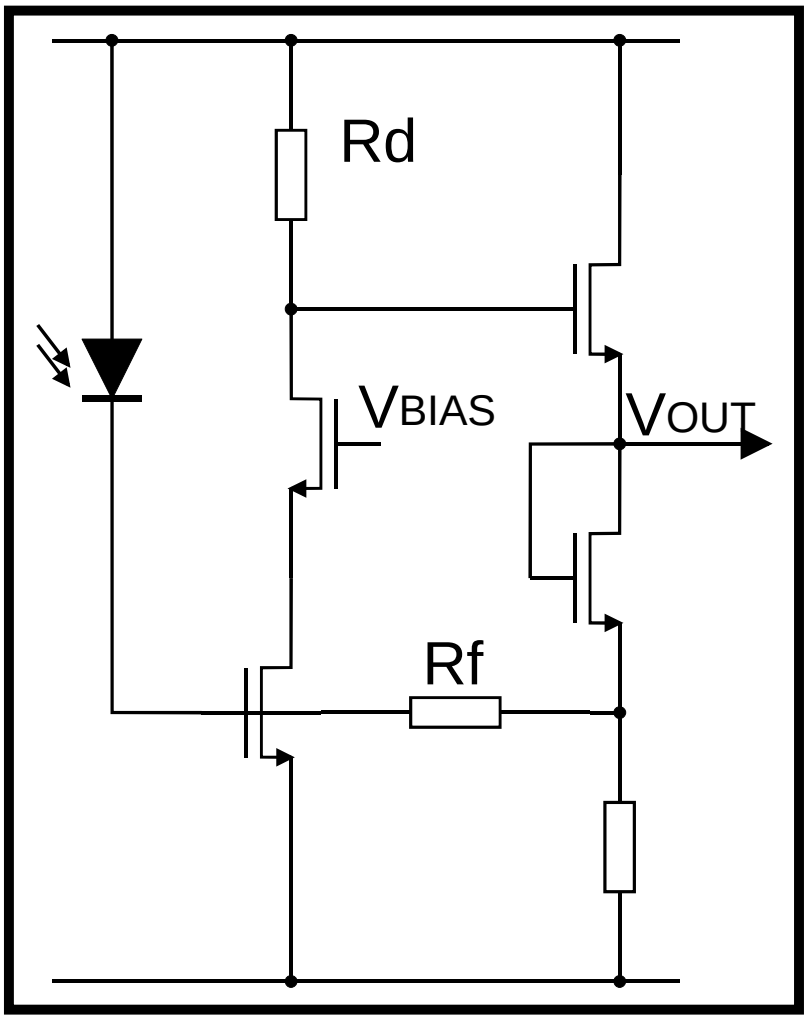


Fiber-Optic Receivers

PIN-Preamplifier:

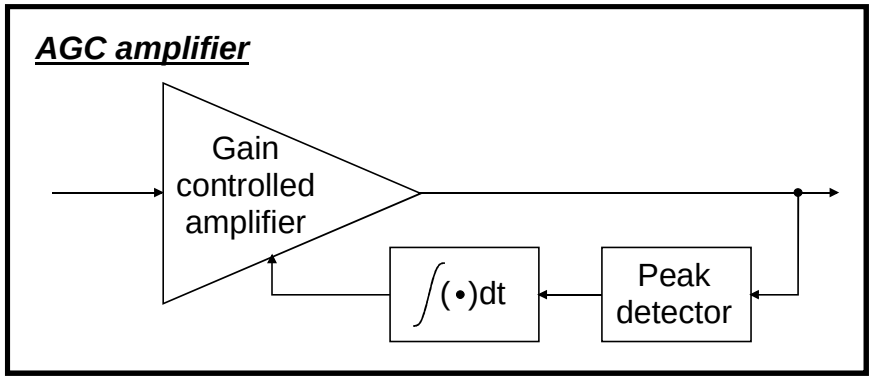
- Amplifies the week photo current with minimum added noise
- The feedback resistance:
  - Controls the gain
  - Controls the bandwidth
  - Influences the noise:

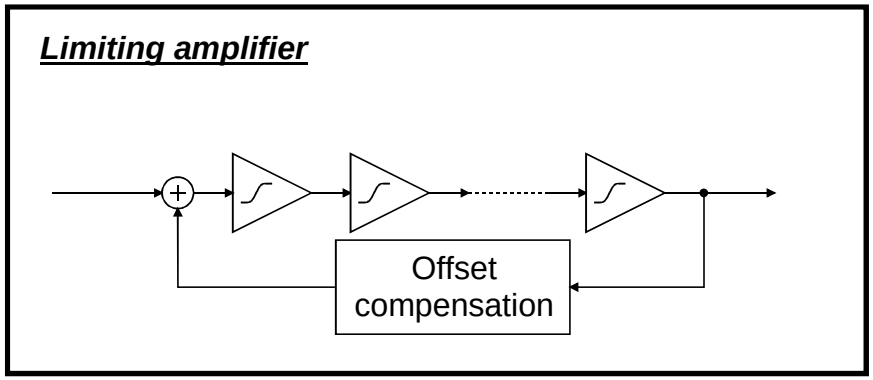
$$S(f) = \frac{4kT}{R_f} + 4kT \cdot \left[\Gamma g_m + \frac{1}{R_d} \right] \cdot \left(\frac{\omega C_T}{g_m} \right)^2$$



Limiting and AGC amplifiers

- Limiting and AGC amplifiers:
  - Required to amplify the PIN-preamplifier signal to full logic levels
- AGC amplifiers adapt the gain to the signal level:
  - For large input signals, avoids overdriving the amplifying stages or the following circuit
  - For small input signals, the gain is maximized reducing the amplifier noise contribution
- Limiting Amplifiers:
  - Use the amplifier intrinsic non-linearity to avoid overdrive
  - Noise is minimized by always using maximum gain
  - Cascades of low gain stages are often used to achieve high gain-bandwidth products
- Both type of amplifiers tend to be fully differential to maximize noise rejection





Clock Recovery

- Clock recovery circuits are used to extract the serial clock information form the serial data
- PLL's with nonlinear Phase Detectors are required to lock on the data stream:
  - Narrow band PLL's have the ability to reject the data jitter and still keep track of slow phase fluctuations
  - PLL's can be implemented to ensure optimum data sampling
- The clock recovery and retiming circuits ensure correct conversion between the "analogue" signal and the binary levels